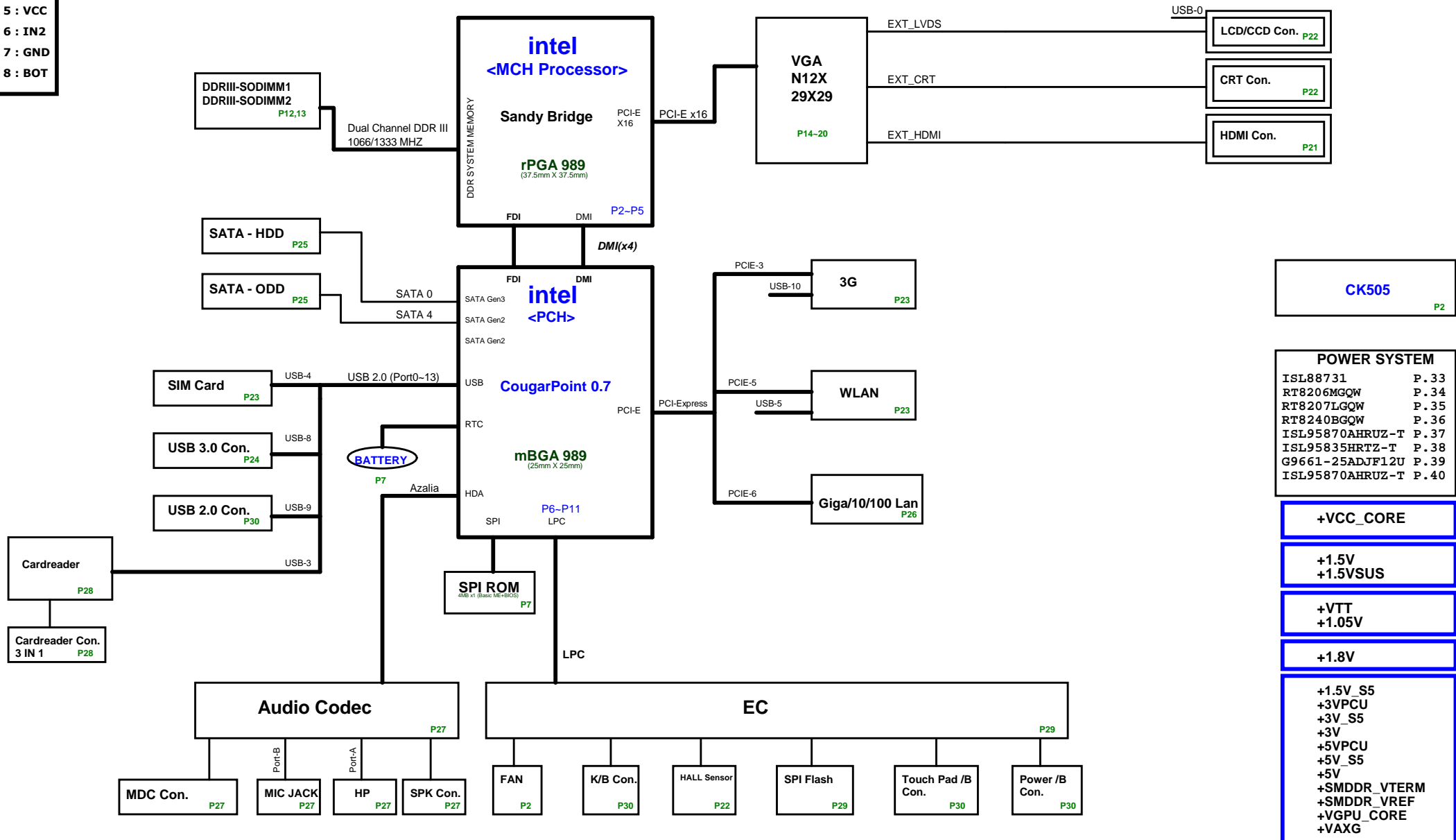


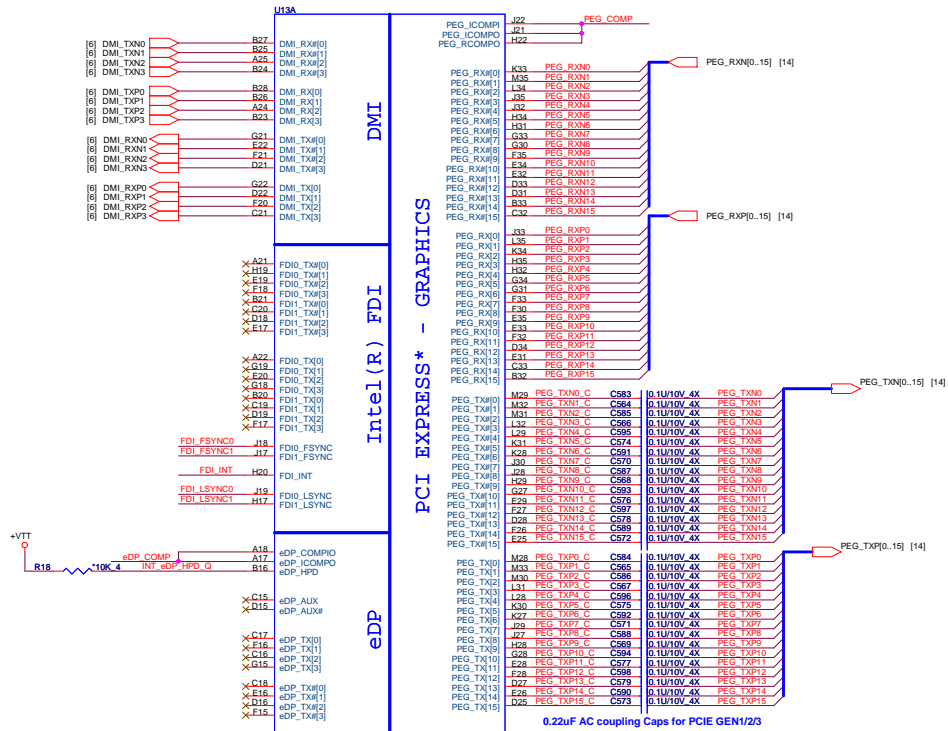
BLBD Block Diagram

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : GND
LAYER 5 : VCC
LAYER 6 : IN2
LAYER 7 : GND
LAYER 8 : BOT

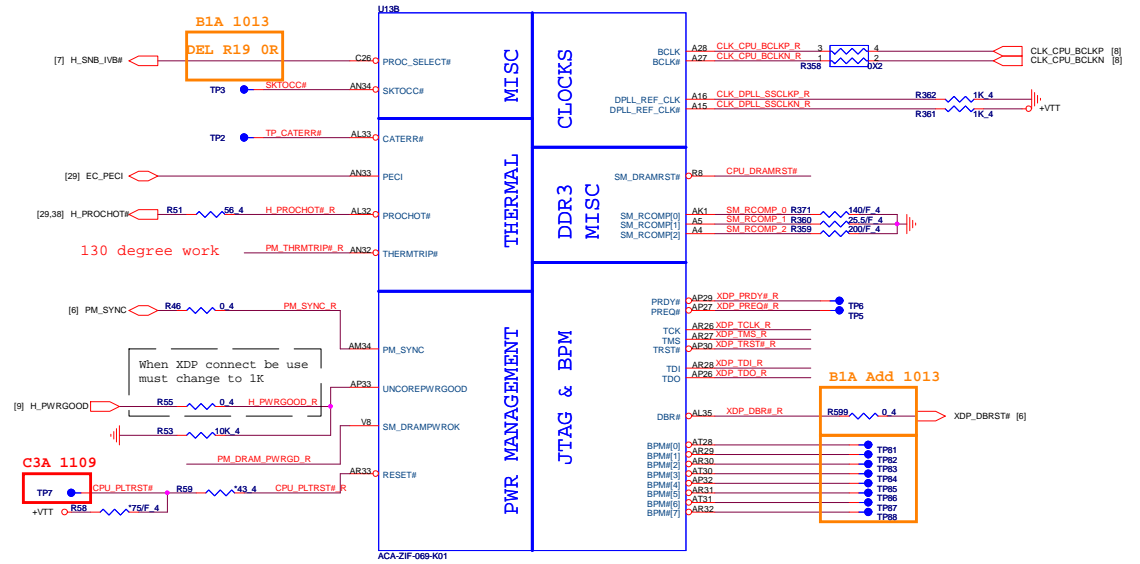


Sandy Bridge Processor (DMI,PEG,FDI)

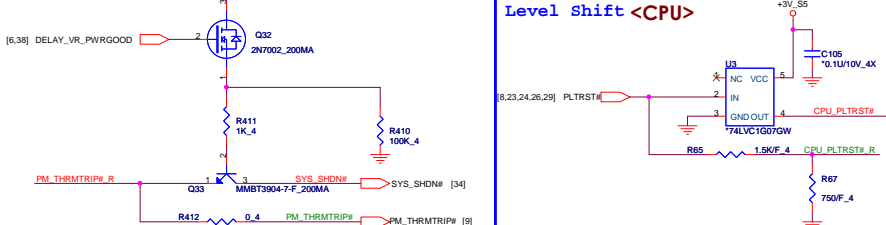


Sandy Bridge Processor (CLK,MISC,JTAG)

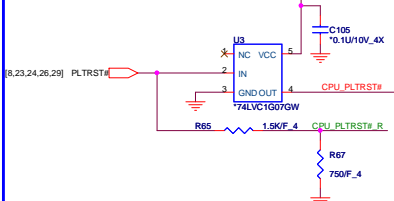
SNB_IVB# N.A at SNB EDS #27637 0.7v1



Thermal Trip

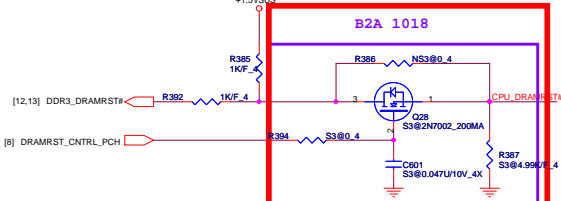


Level Shift <CPU>

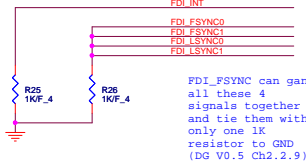
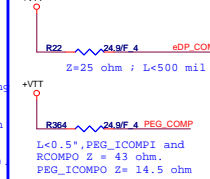


S3 Power Reduction

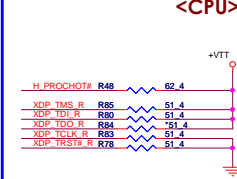
C3A 1118 (討論結果:保留S3)



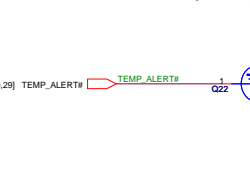
FDI Disabling (Discrete Only)
[CPU]

DP & PEG Compensat
+VII

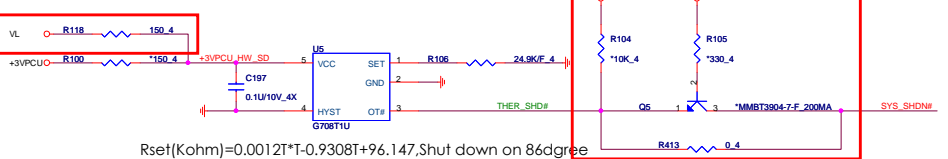
Processor pull-up



CPU FAN CTRL <THC/THV>



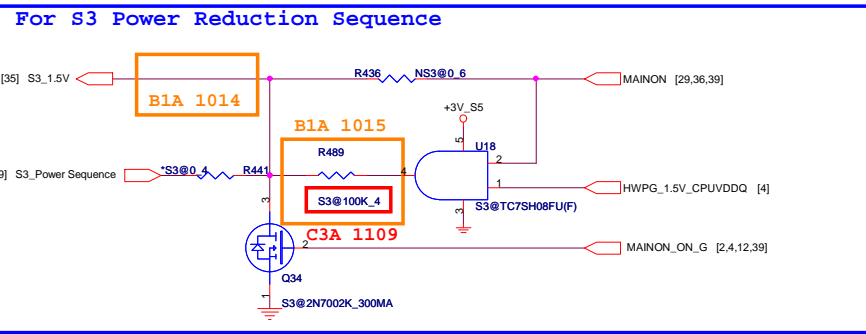
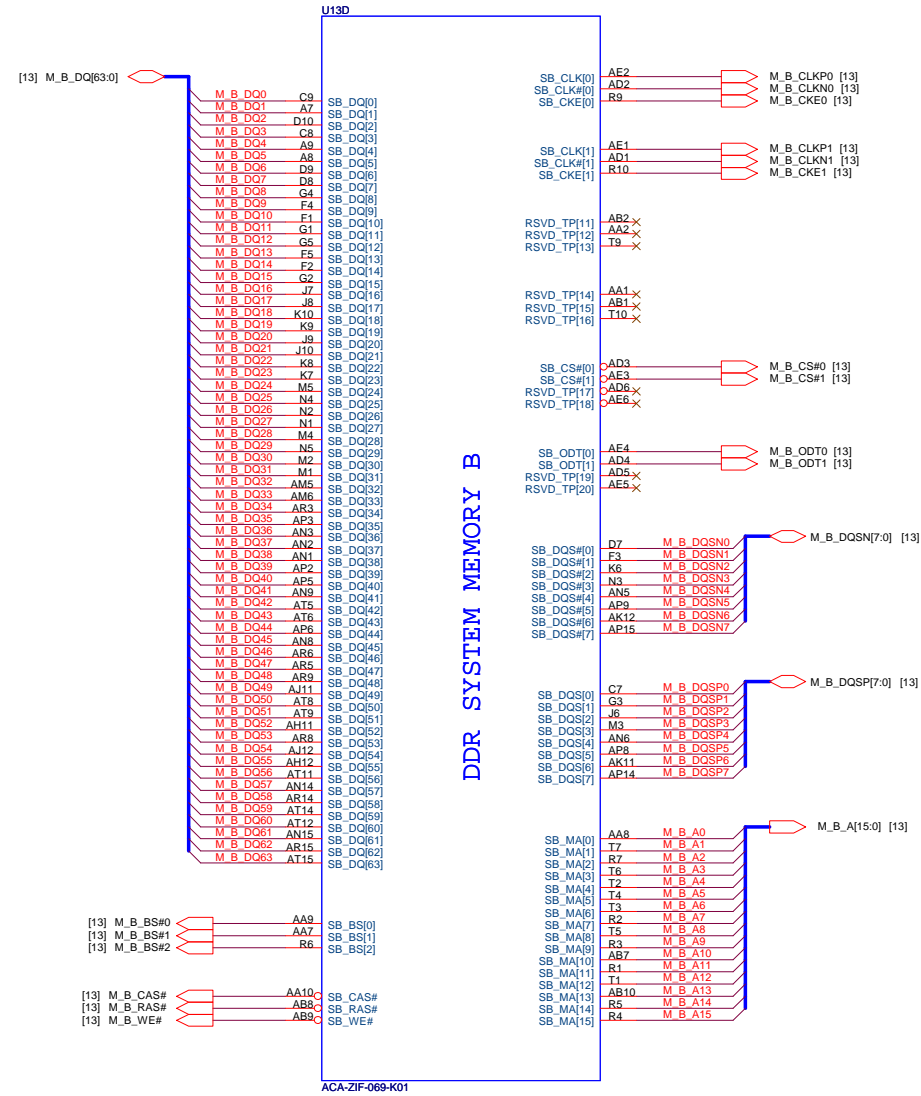
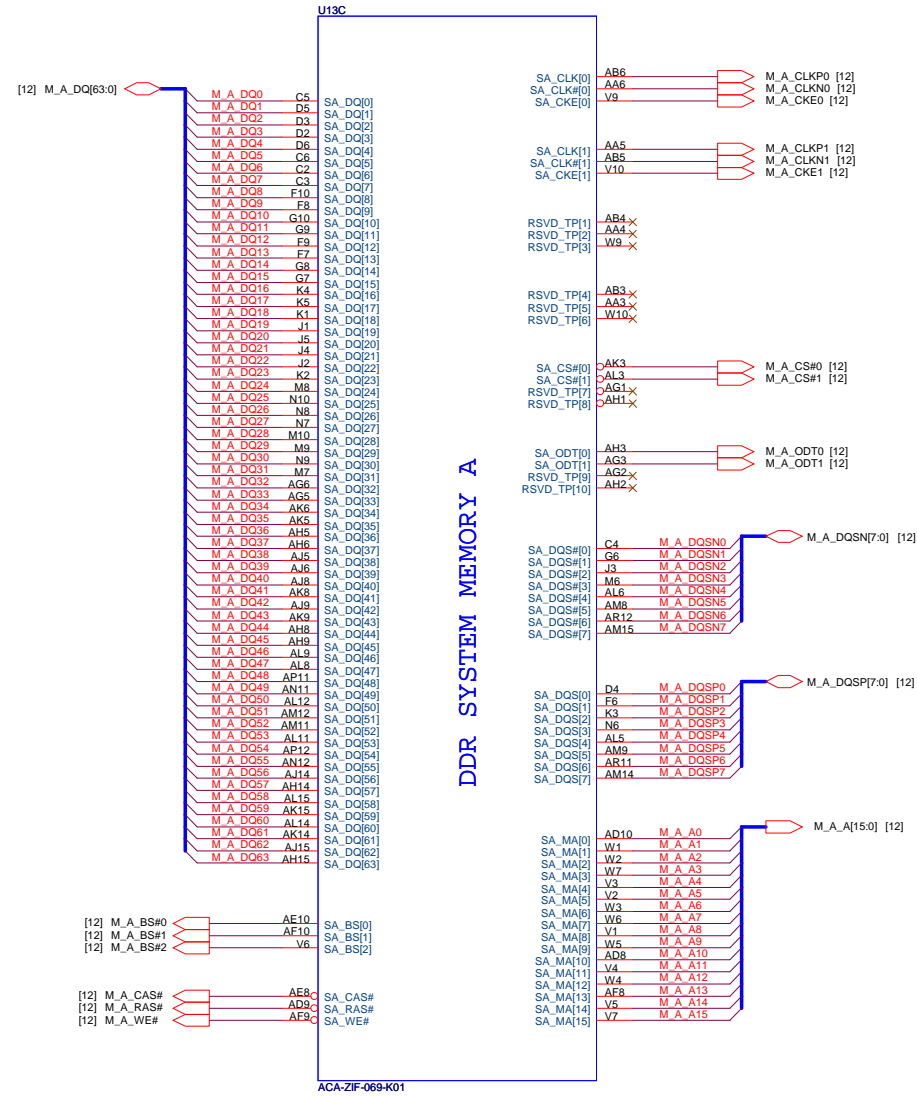
CPU Thermal sensor / MB Local TEMP

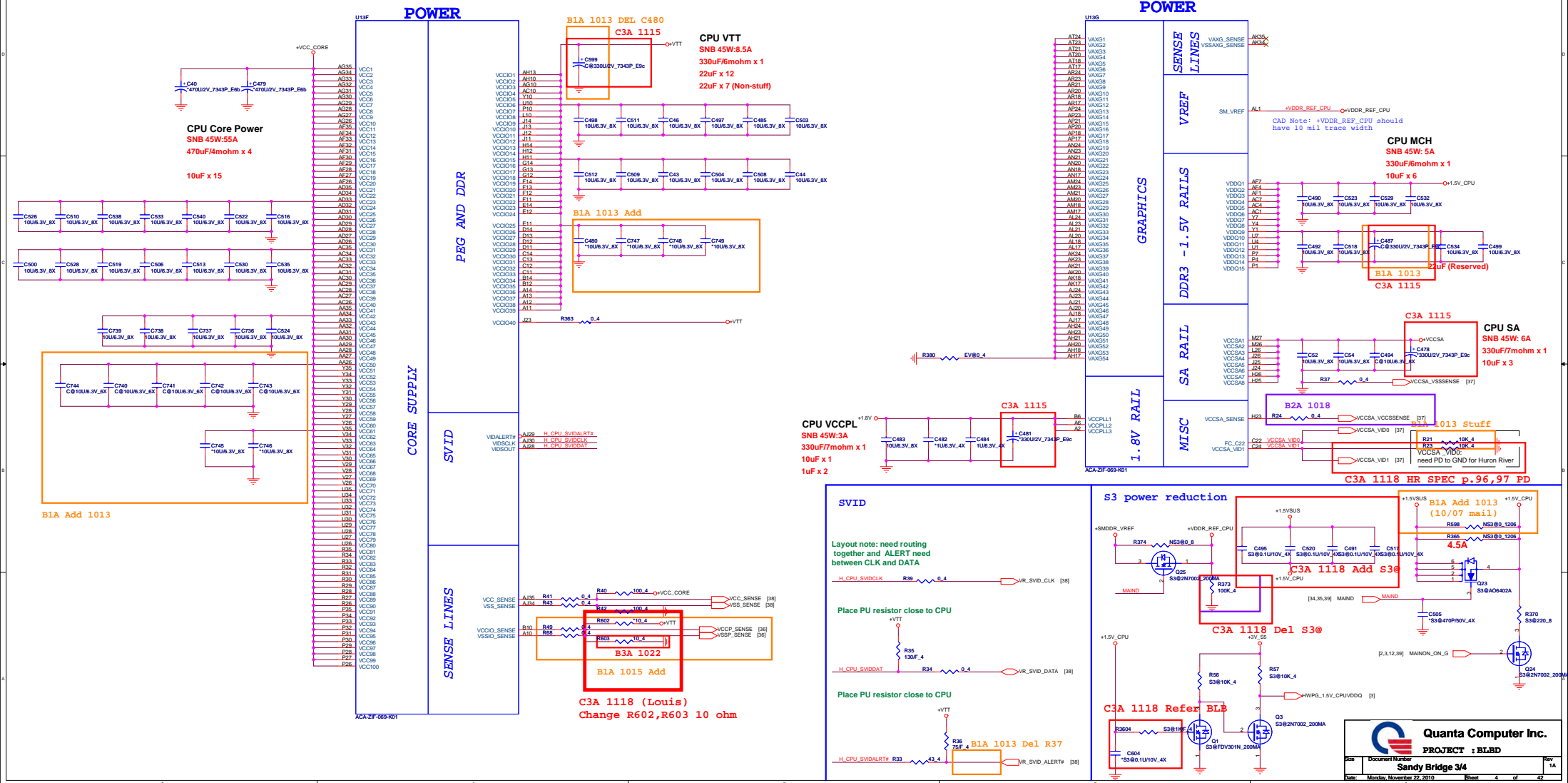


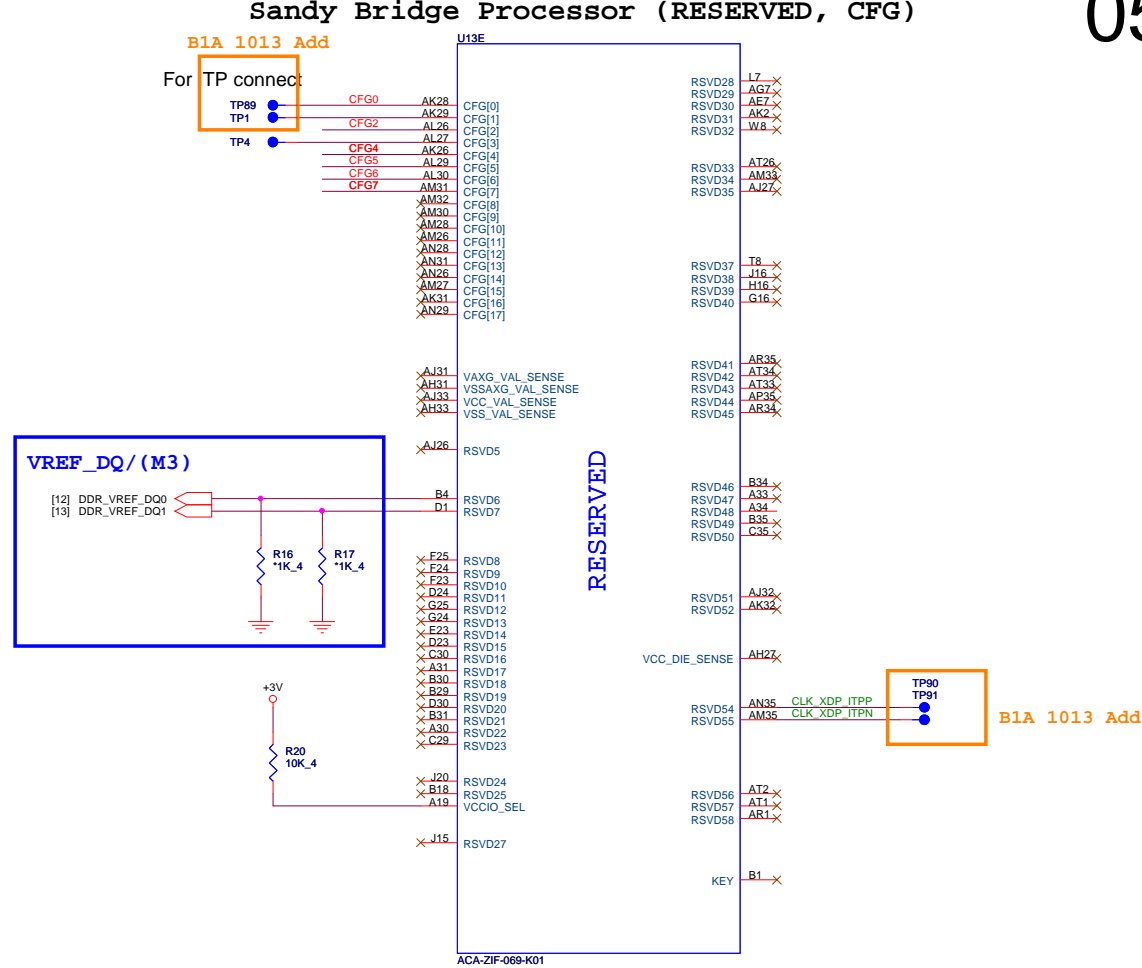
C3A 1116 mail 1018 for cost down Q5

Sandy Bridge Processor (DDR3)

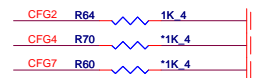
03







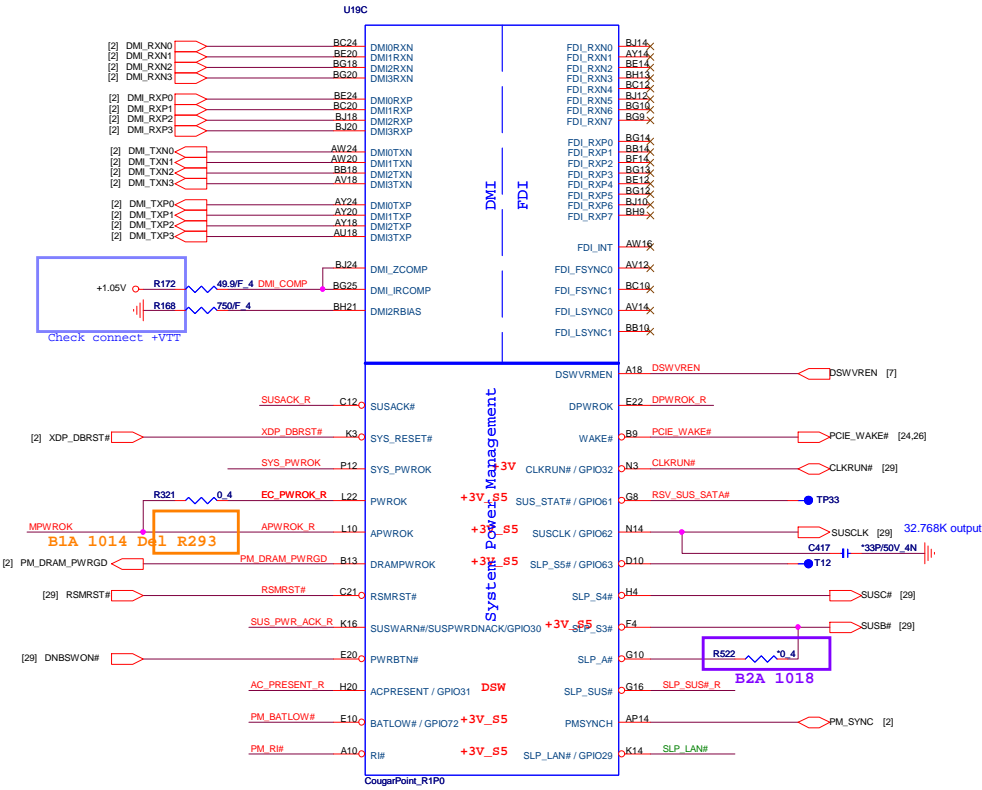
The CFG signals have a default value of '1' if not terminated on the board.



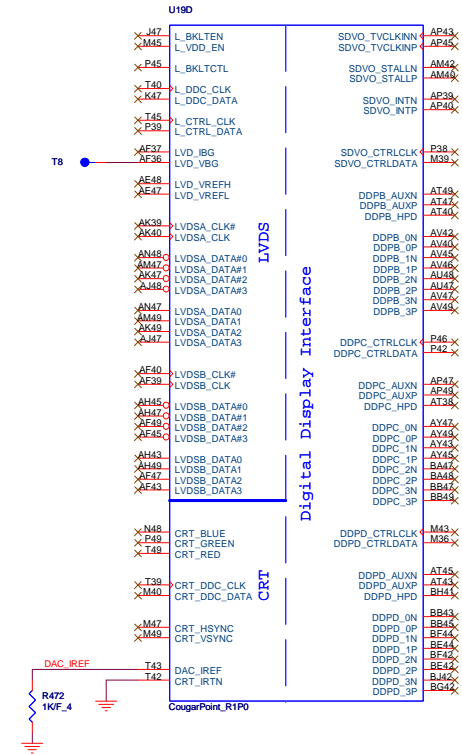
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

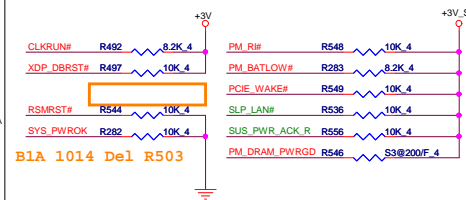
Cougar Point (DMI, FDI, PM)



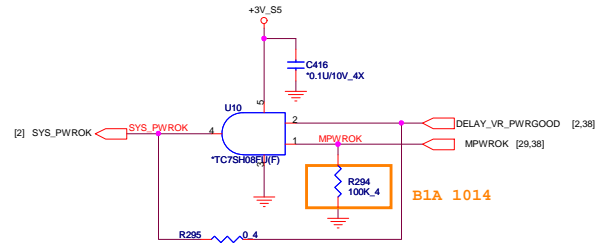
Cougar Point (LVDS, DDI)



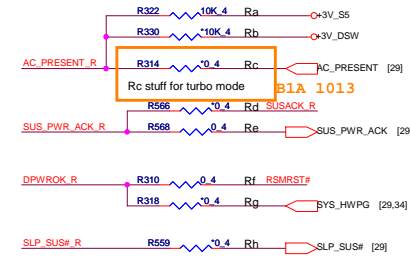
PCH Pull-high/low(CLG)



System PWR_OK(CLG)

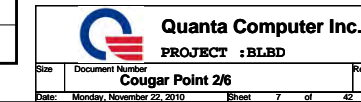


Deep Sx



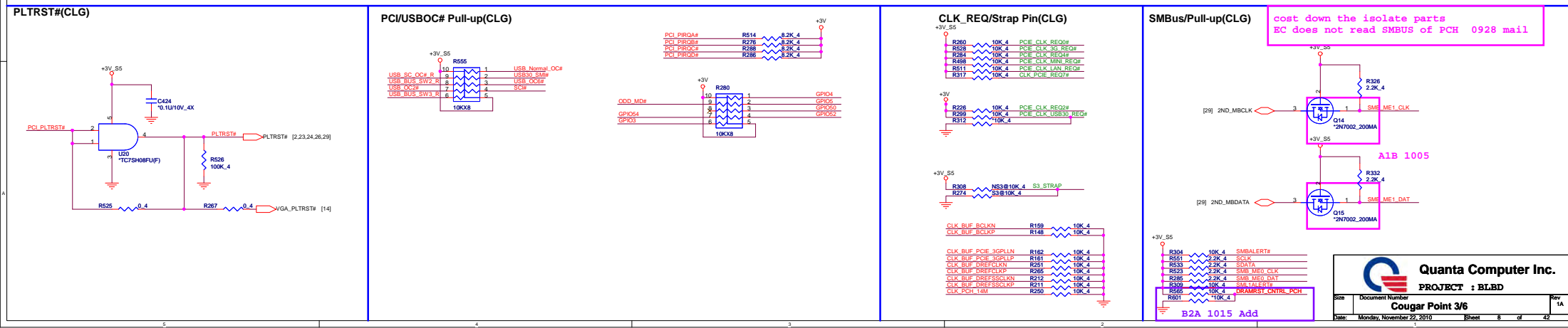
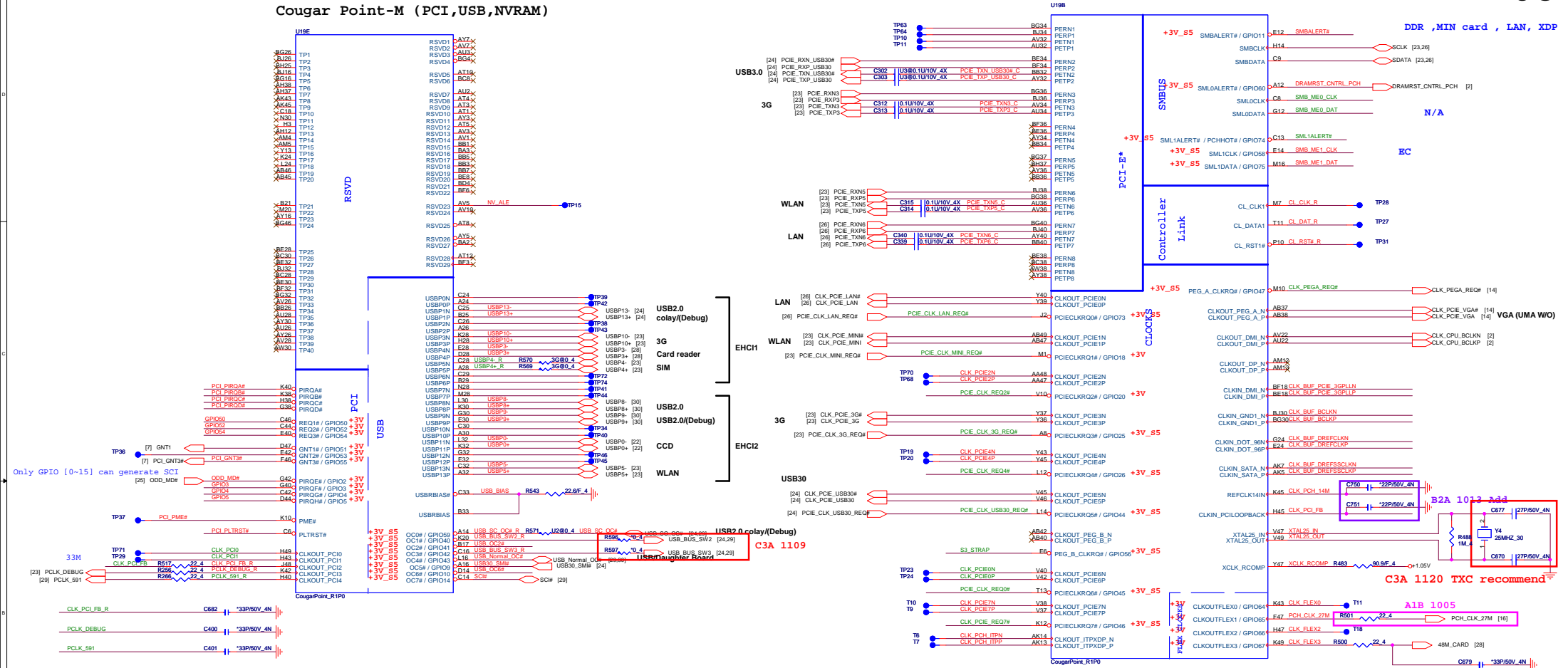
Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

07



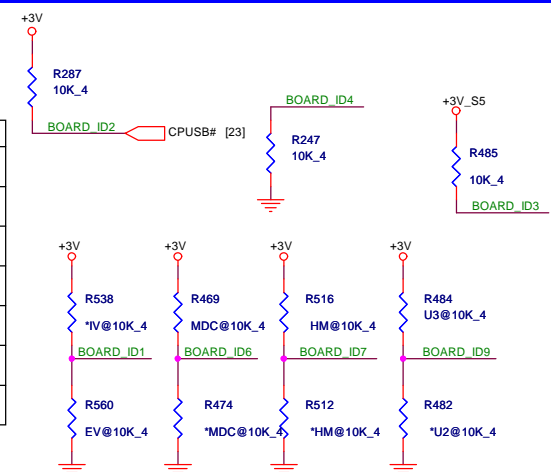
Cougar Point-M (PCI-E,SMBUS,CLK)

Cougar Point-M (PCI,USB,NVRAM)

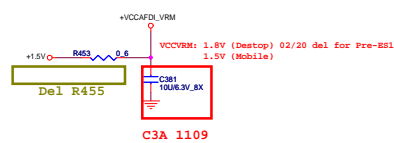
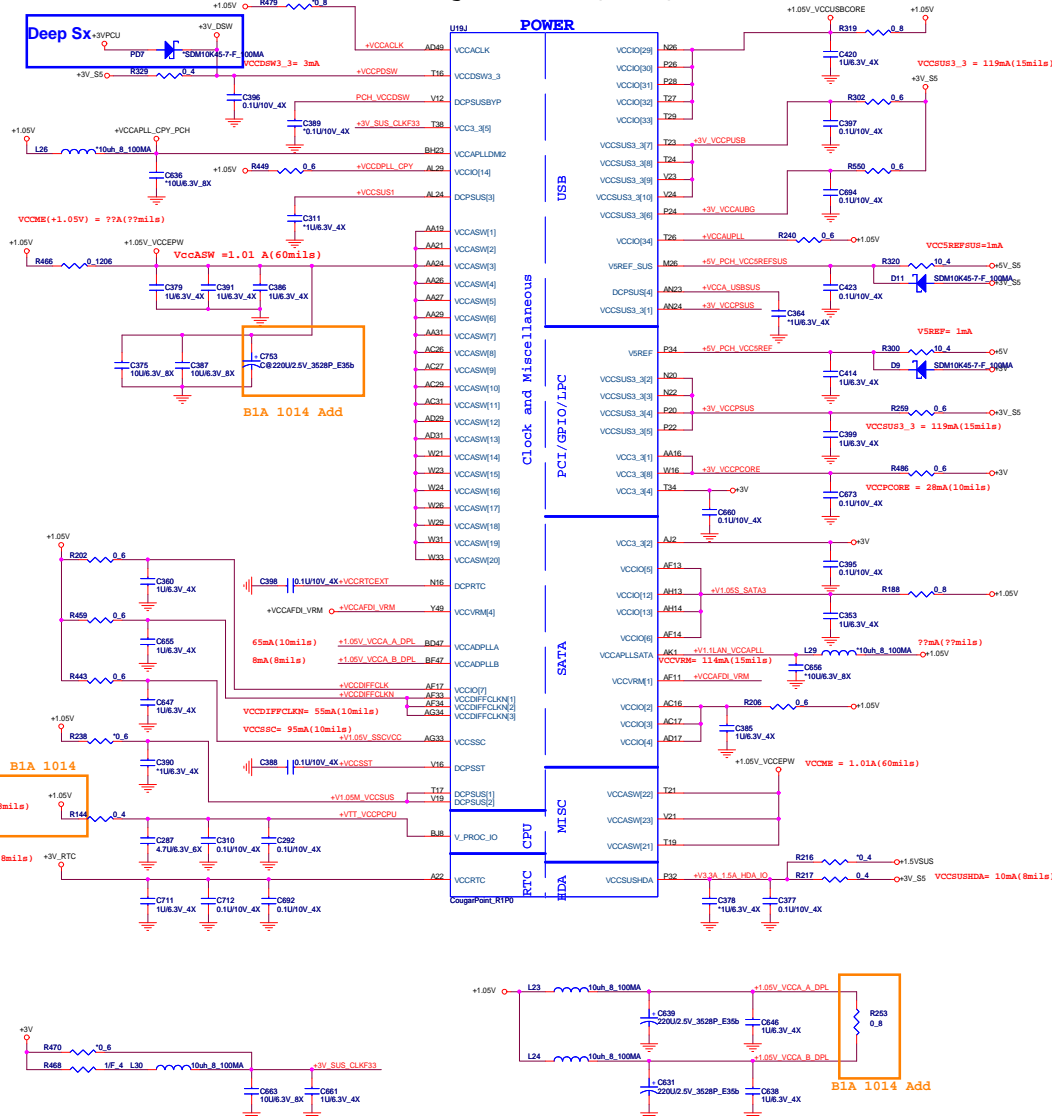




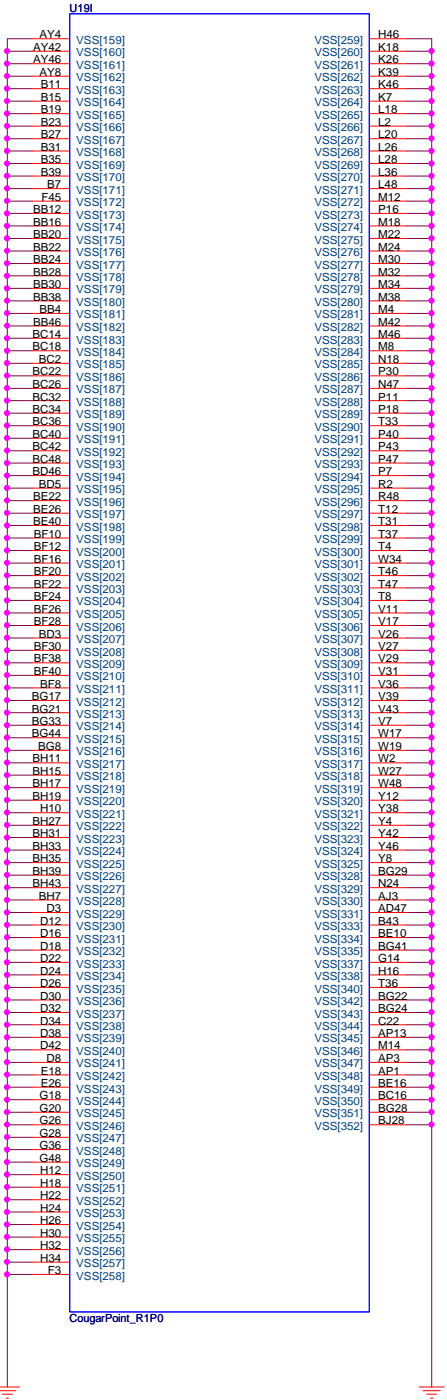
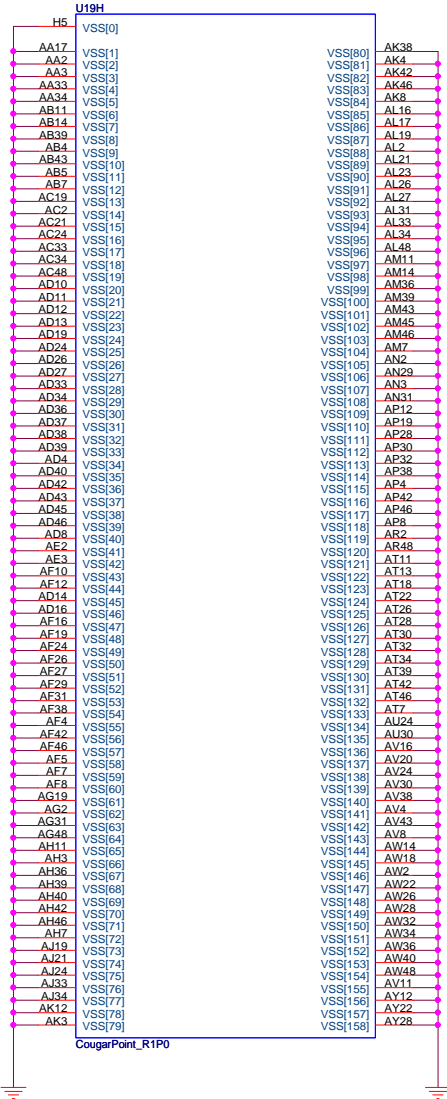
B1A 1014



Cougar Point-M (POWER)

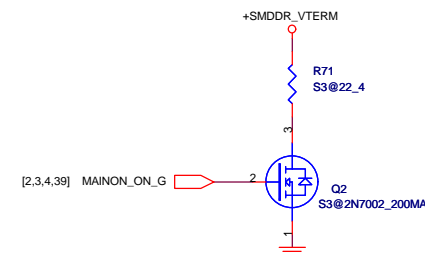


IBEX PEAK-M (GND)





S3 Power Reduction

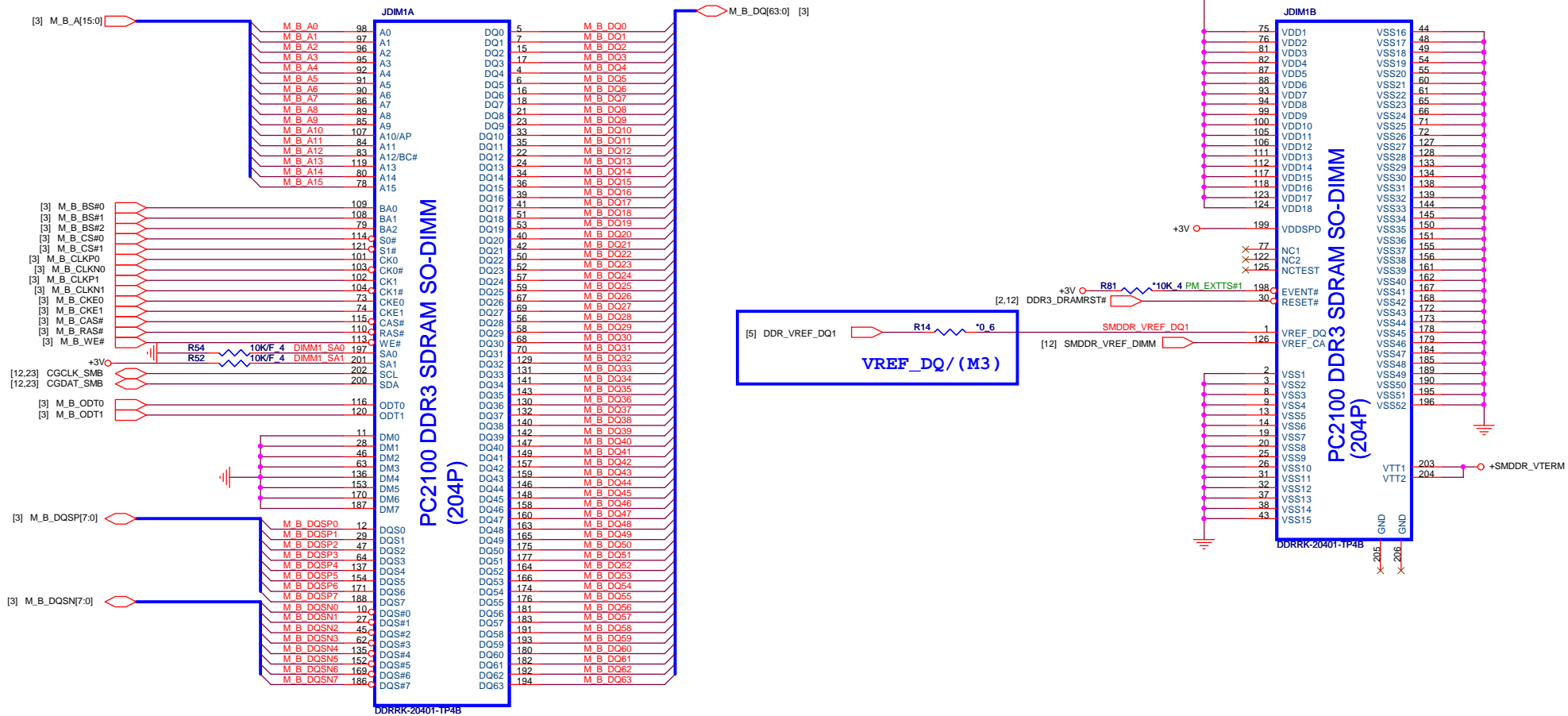


Re	
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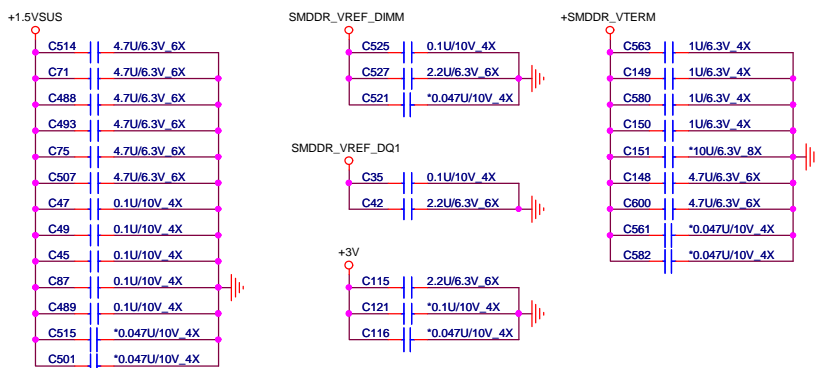
H=8

H=8

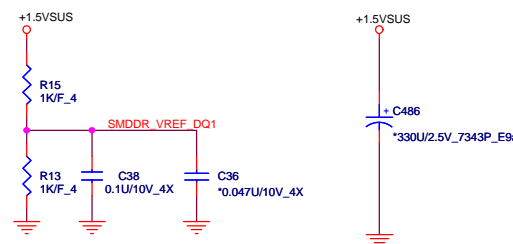
13



Place these Caps near So-Dimm1.

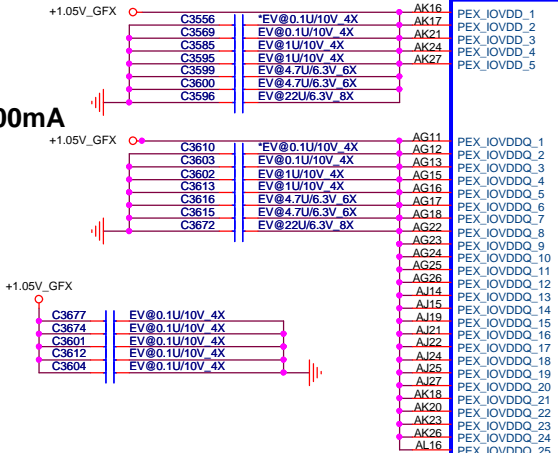


VREF_DQ/ (M1)

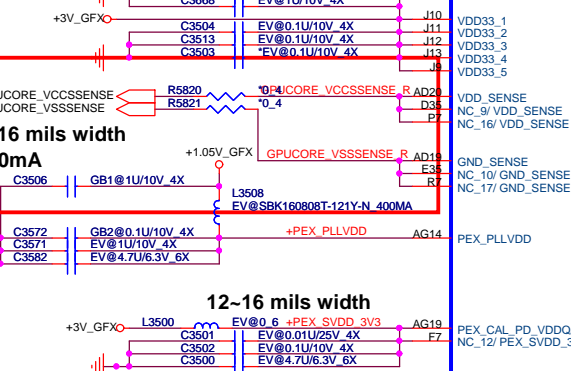


PEX IOVDD+PEX IOVDDQ+PEX PLLVDD >2.2A

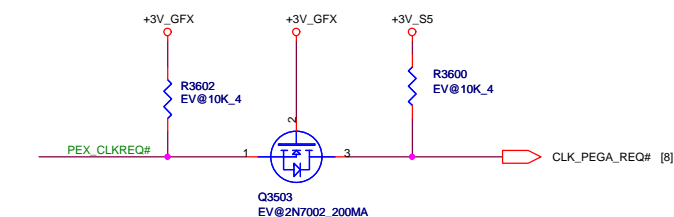
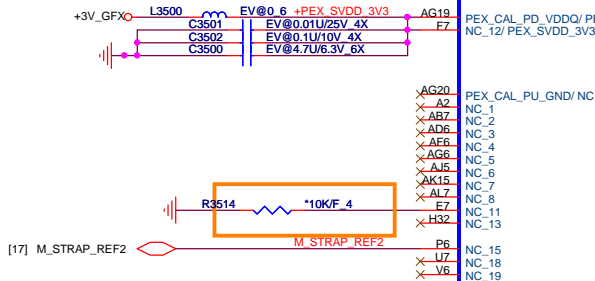
~ 500mA



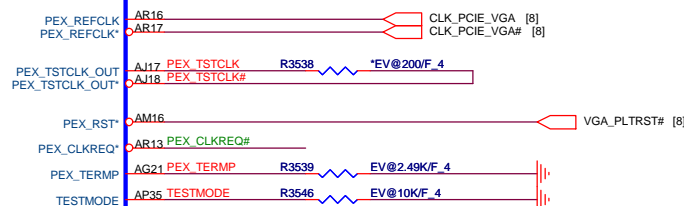
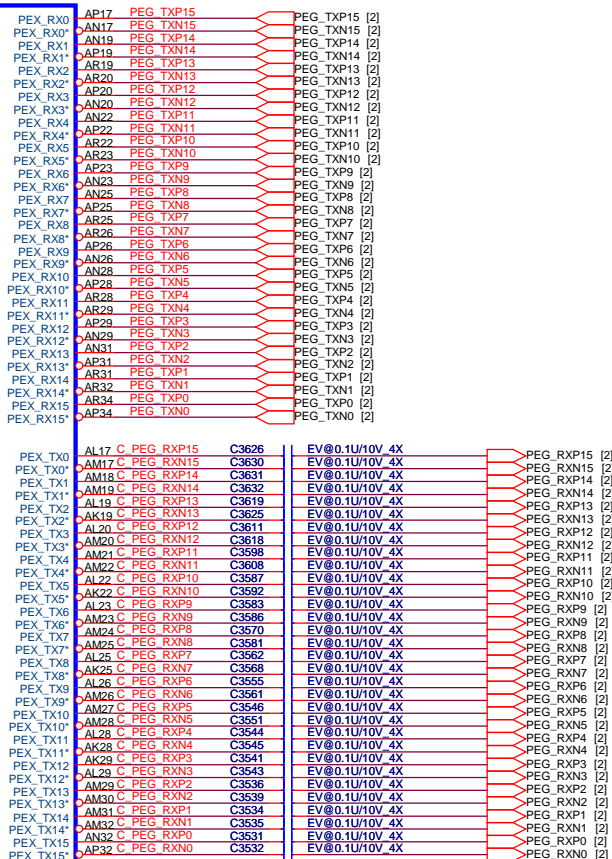
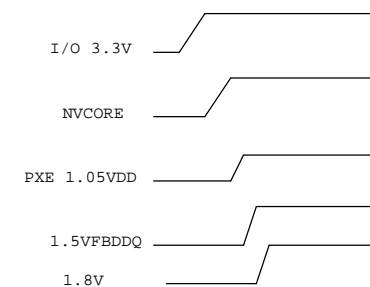
PCI EXPRESS



12~16 mils width

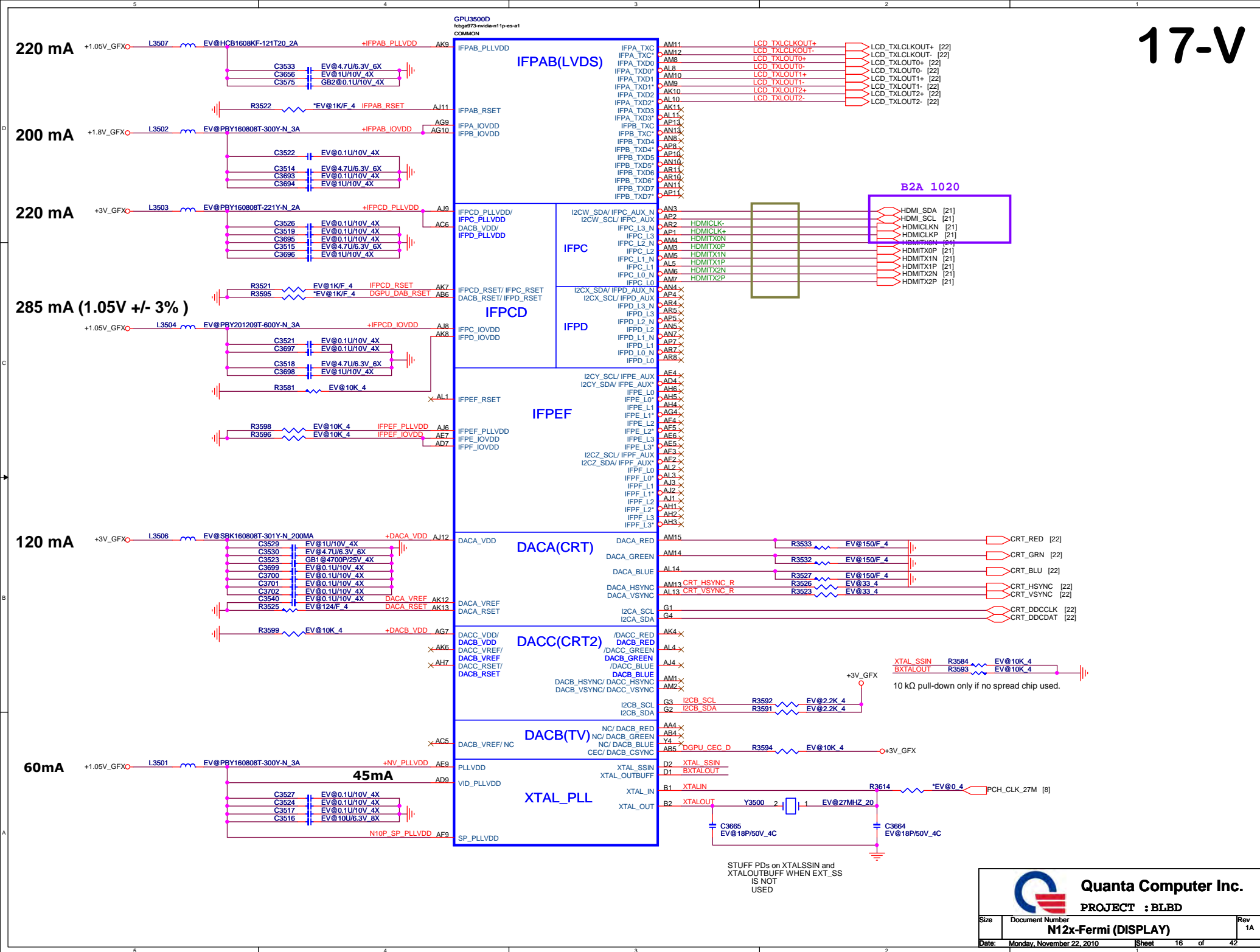


power up sequence

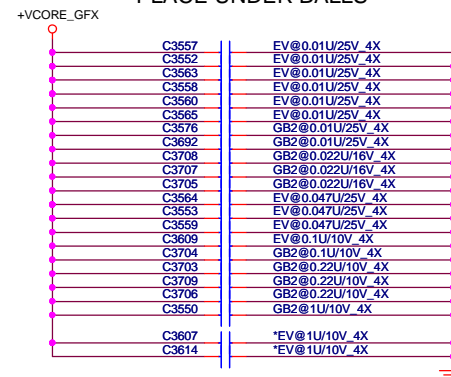




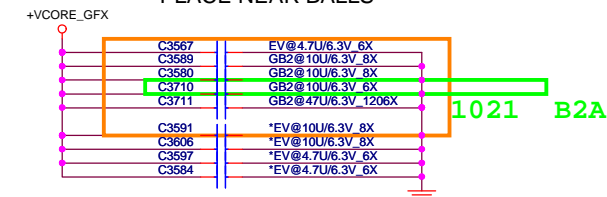
17-V



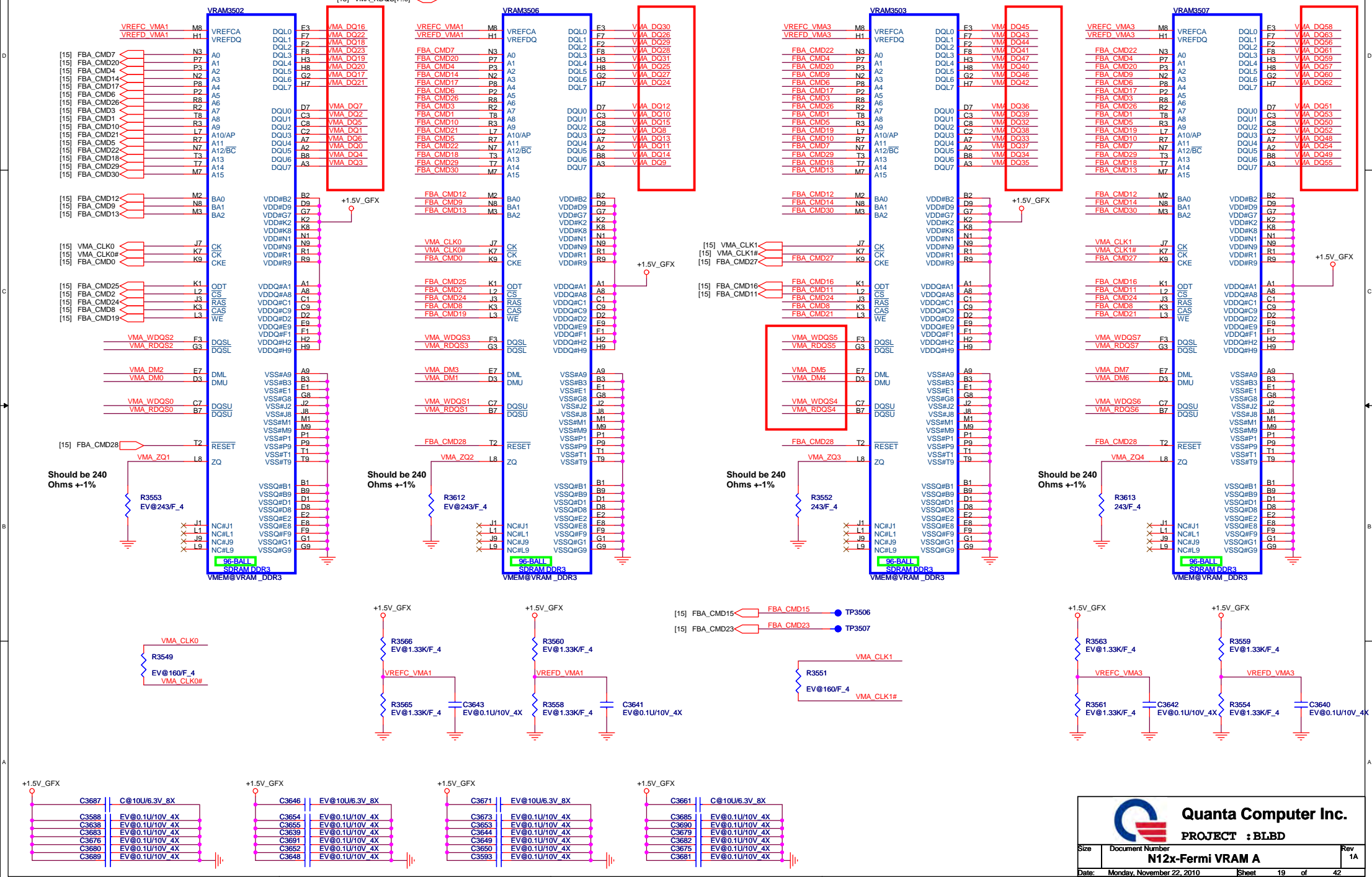
PLACE UNDER BALLS



PLACE NEAR BALLS



CHANNEL A: 256MB/512MB DDR3



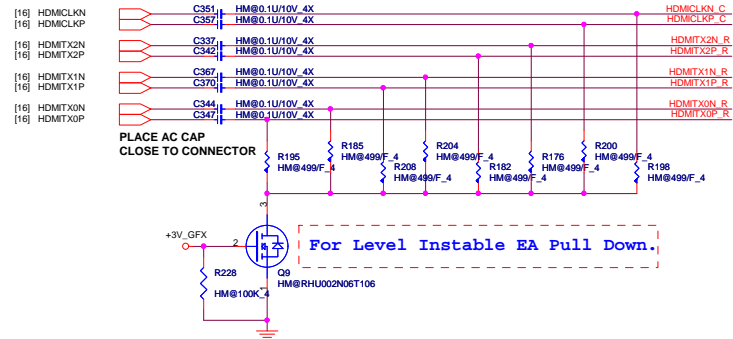


VGA HDMI

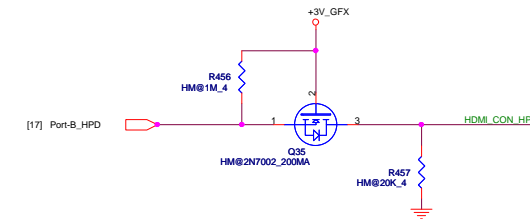
HDMI-passive level shift <HMP/HMG>

HDMI Interface

Angelo 0921

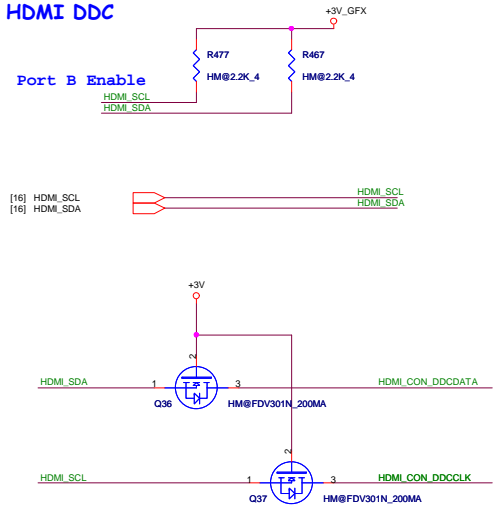


HDMI HPD

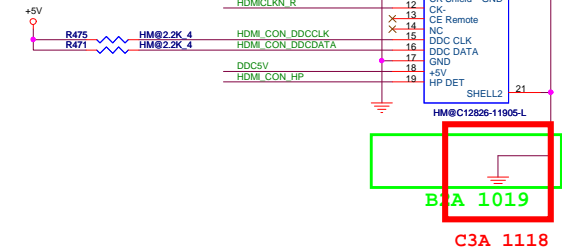
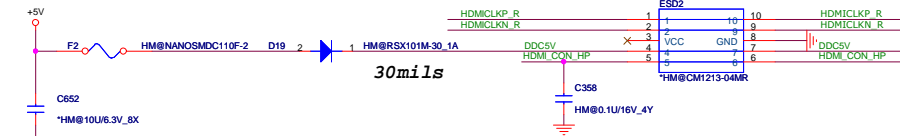
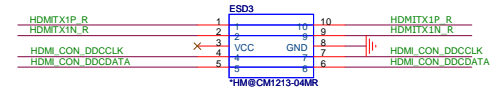
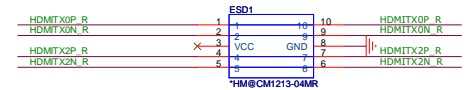
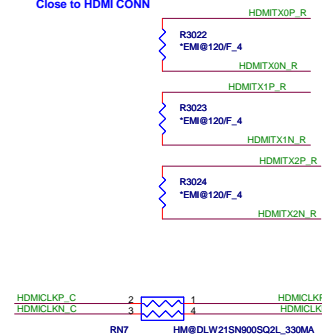


HDMI DDC

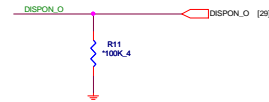
Port B Enable



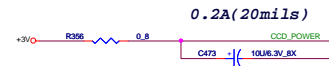
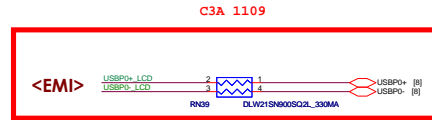
Close to HDMI CONN



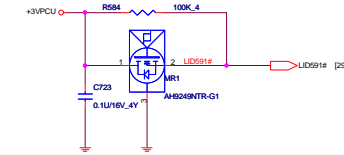
Panel backlight control <LDS>



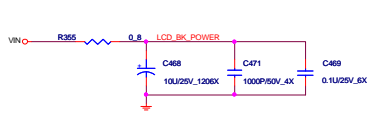
CCD <CCD>



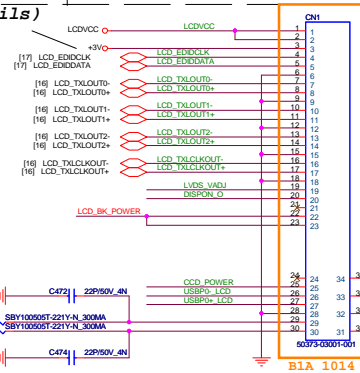
HALL SENSOR&BACK LIGHT SWITCH <HSR>



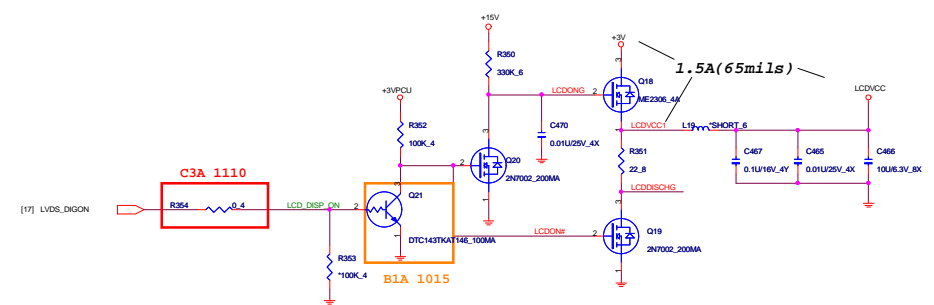
LCD Panel Module <LDS>



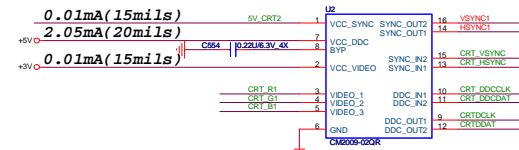
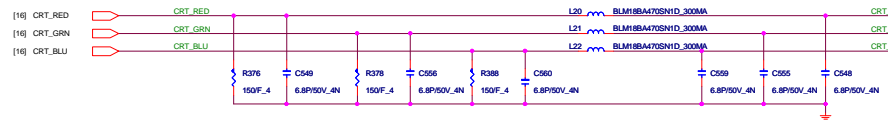
0.3A (20mils)



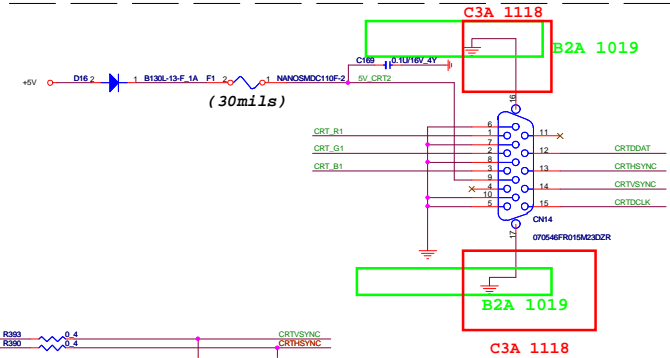
LCD POWER SWITCH <LDS>



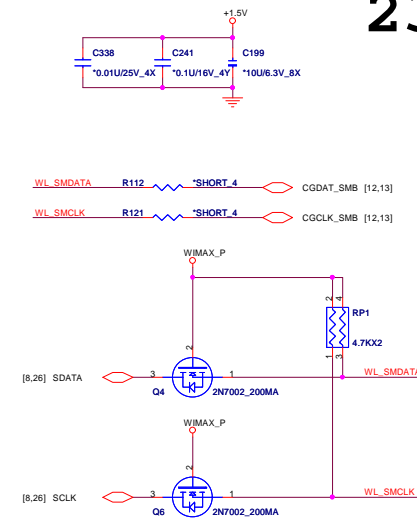
CRT <CRT>



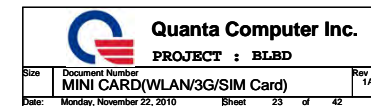
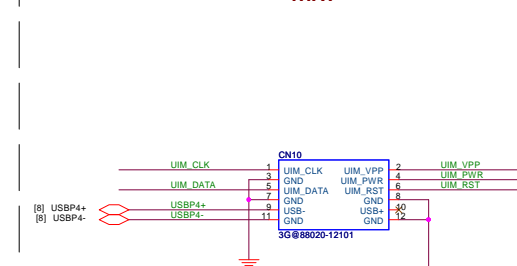
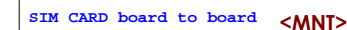
<DPP>

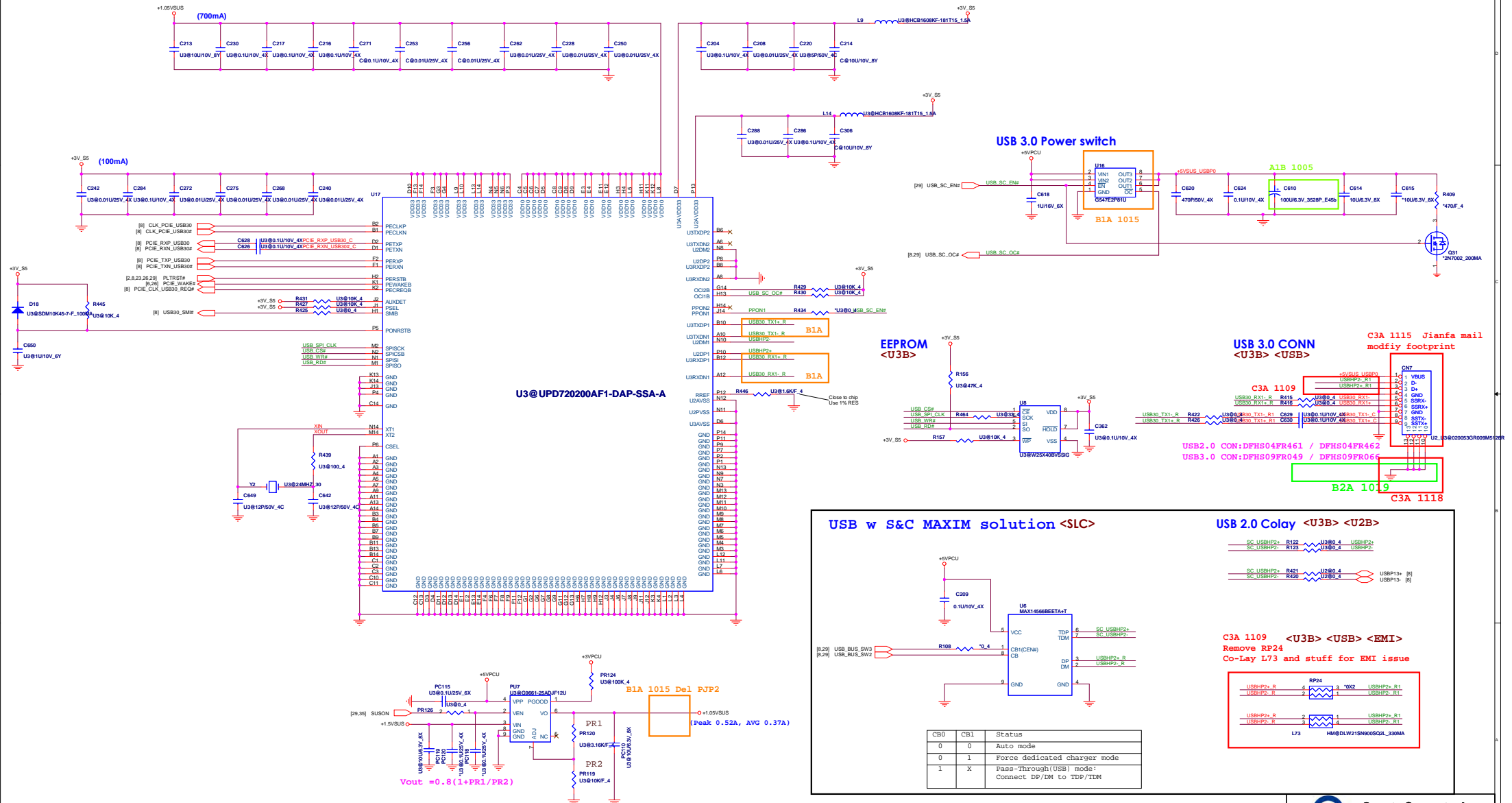


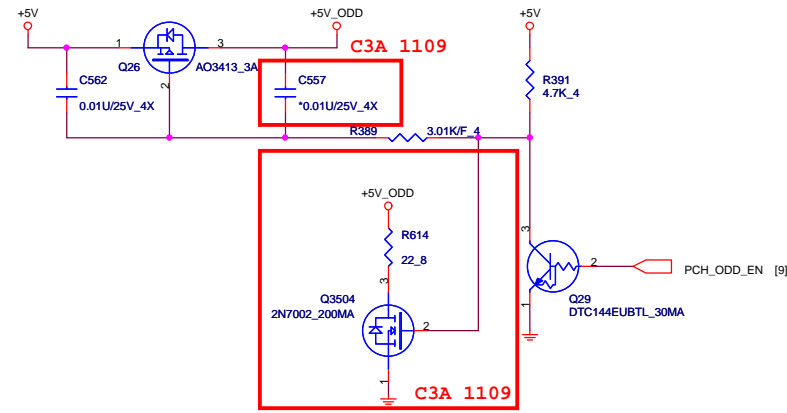
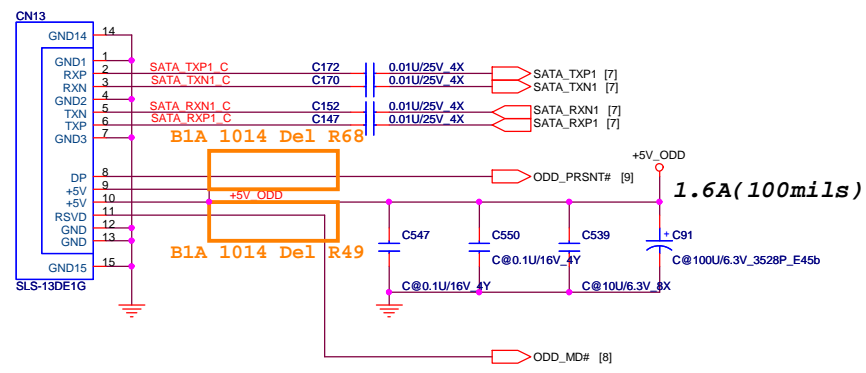
+3V



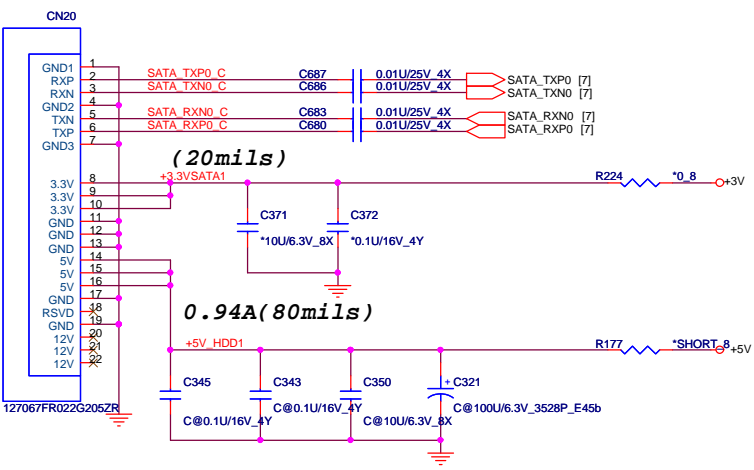
1000



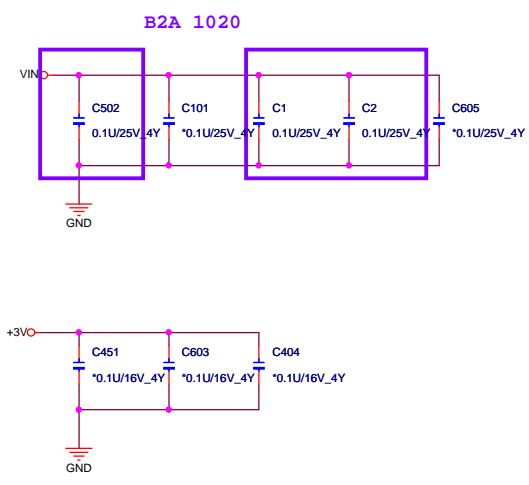




SATA HDD

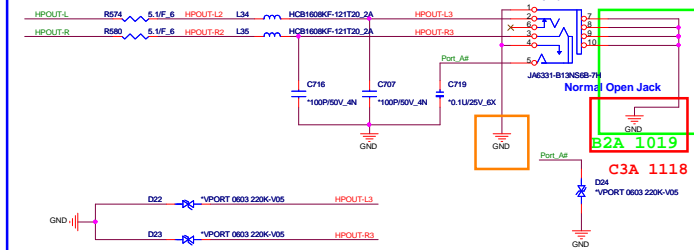


EMI

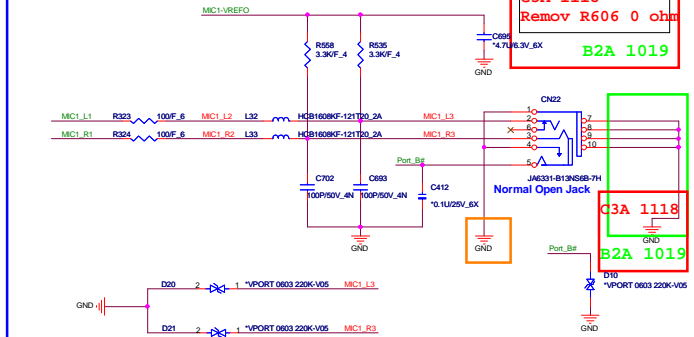


Earphone

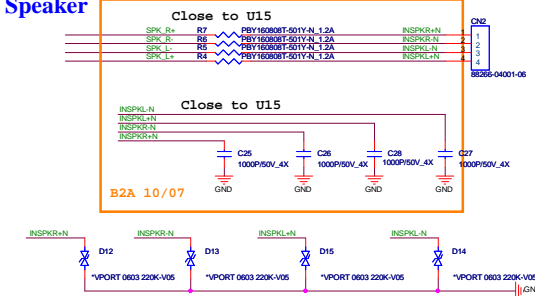
27



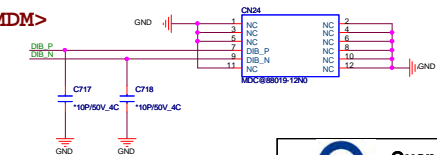
External MIC



Internal Speaker



MDC <MDM>

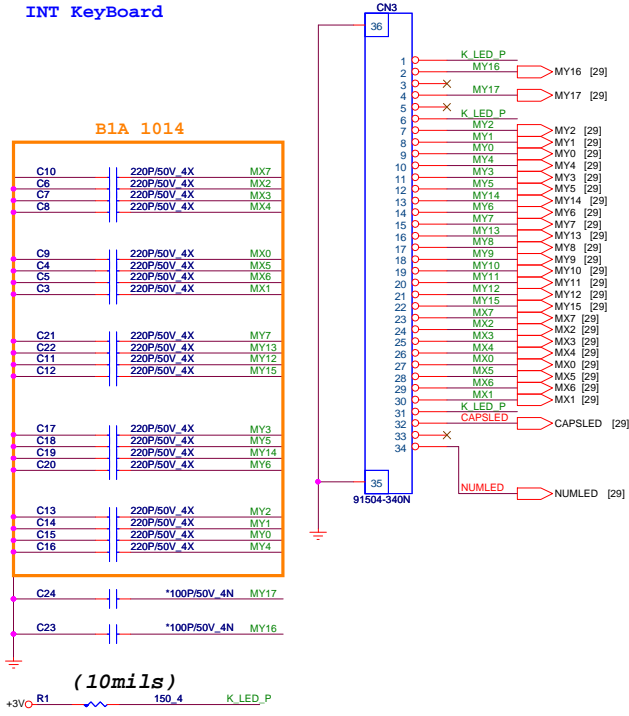


28

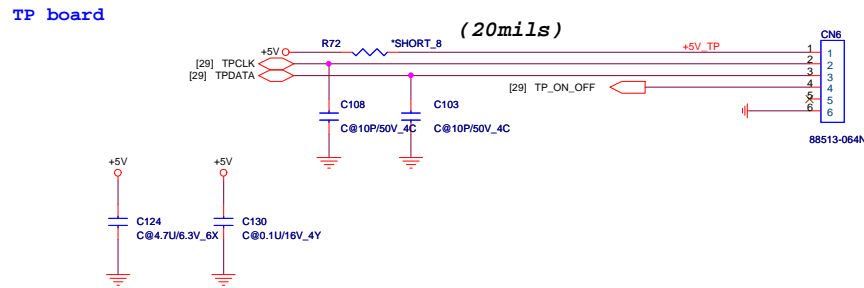


AL005128001 IC CTRL(24P) RTS5128-GRT(QFN)

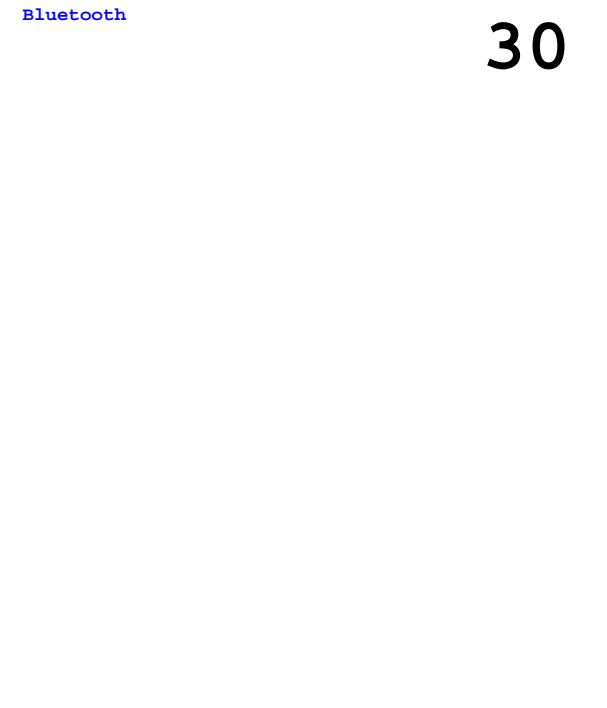
INT Keyboard



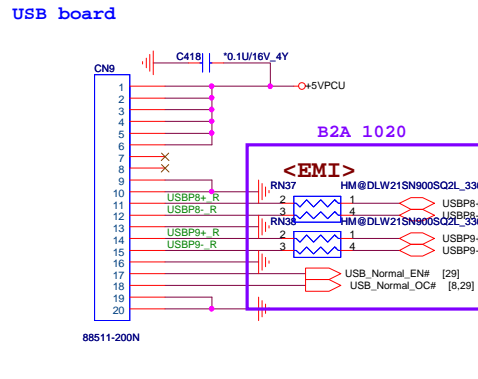
TP board



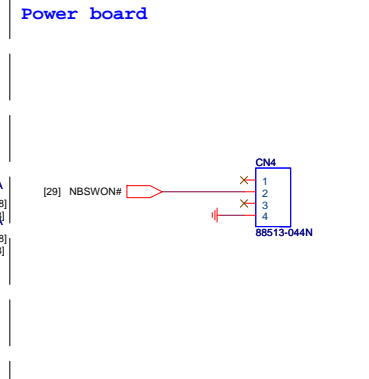
Bluetooth



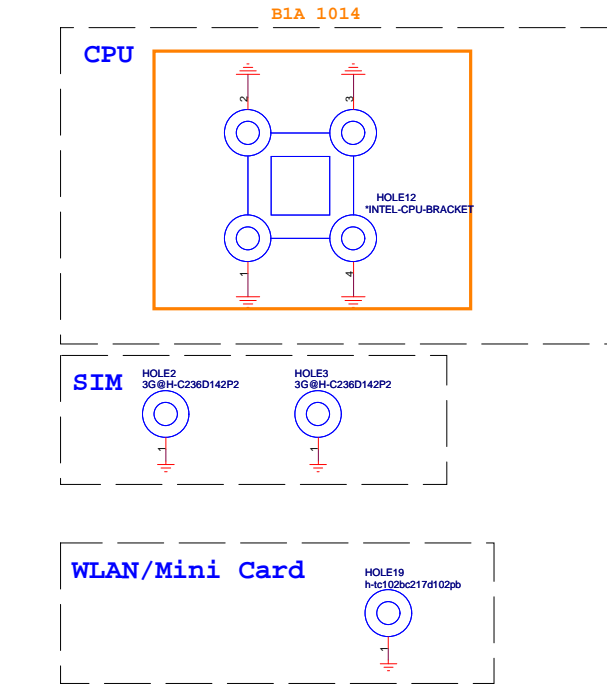
USB board



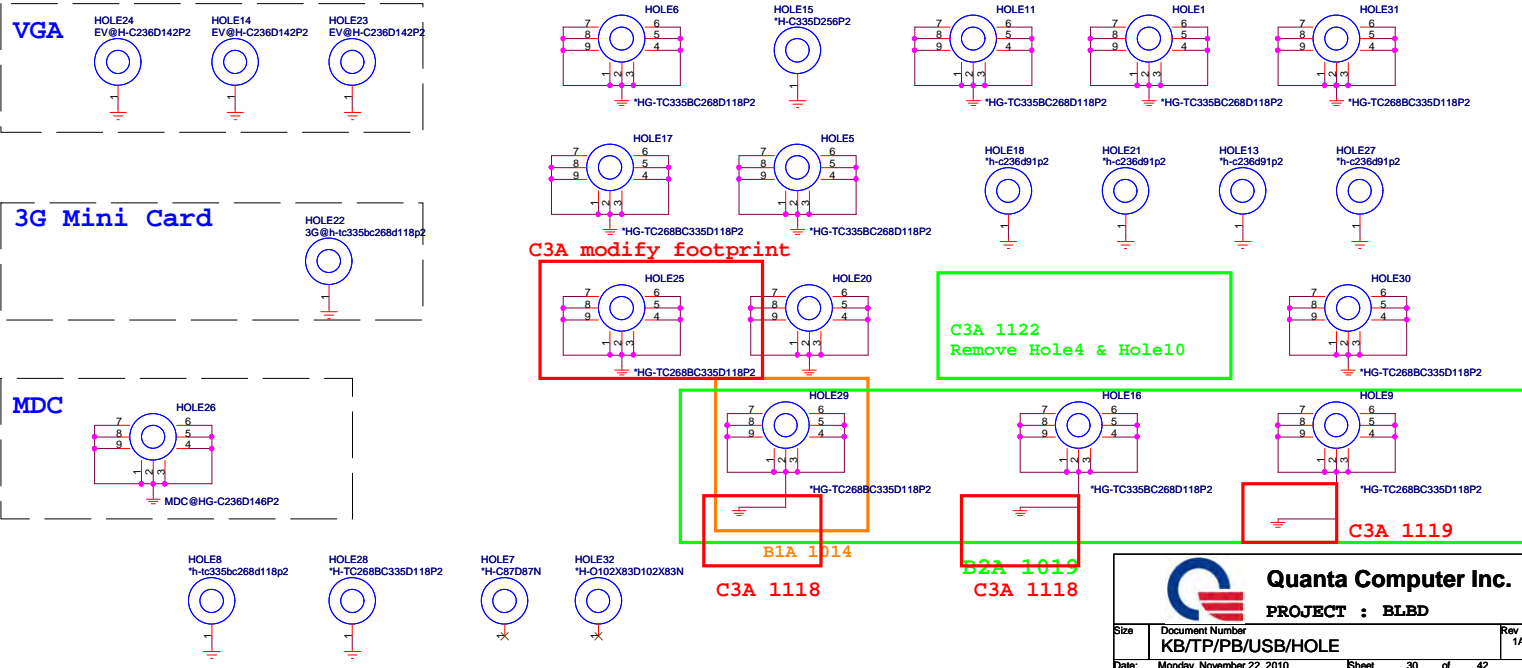
Power board



NUT

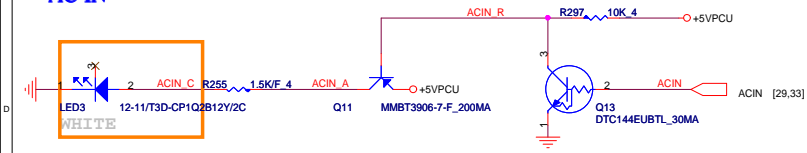


HOLE



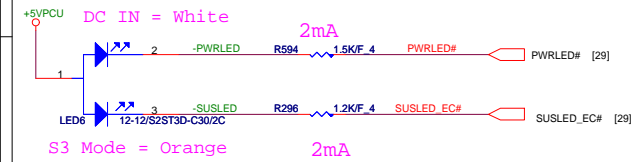
LED

AC-IN

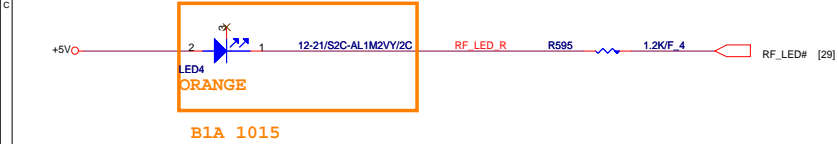


B1A 1015

POWER

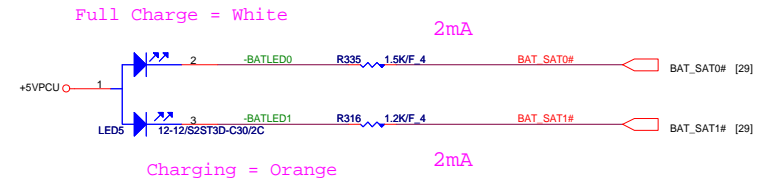


RF LED

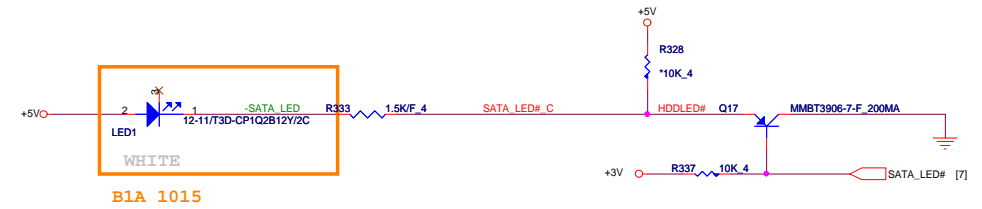
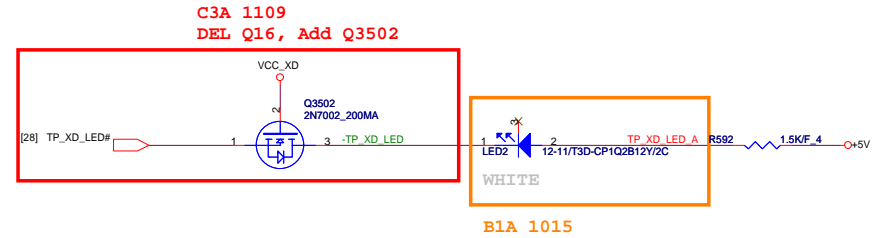


HDD/ODD

BATTERY

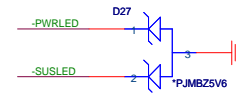


CARDREADER

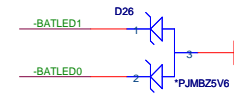


ESD Protect

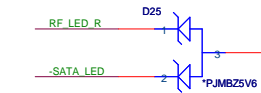
FOR POWER LED



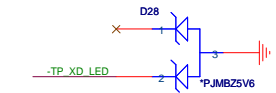
FOR BATTERY LED




FOR HDD/RF LED



FOR CARDREADER LED



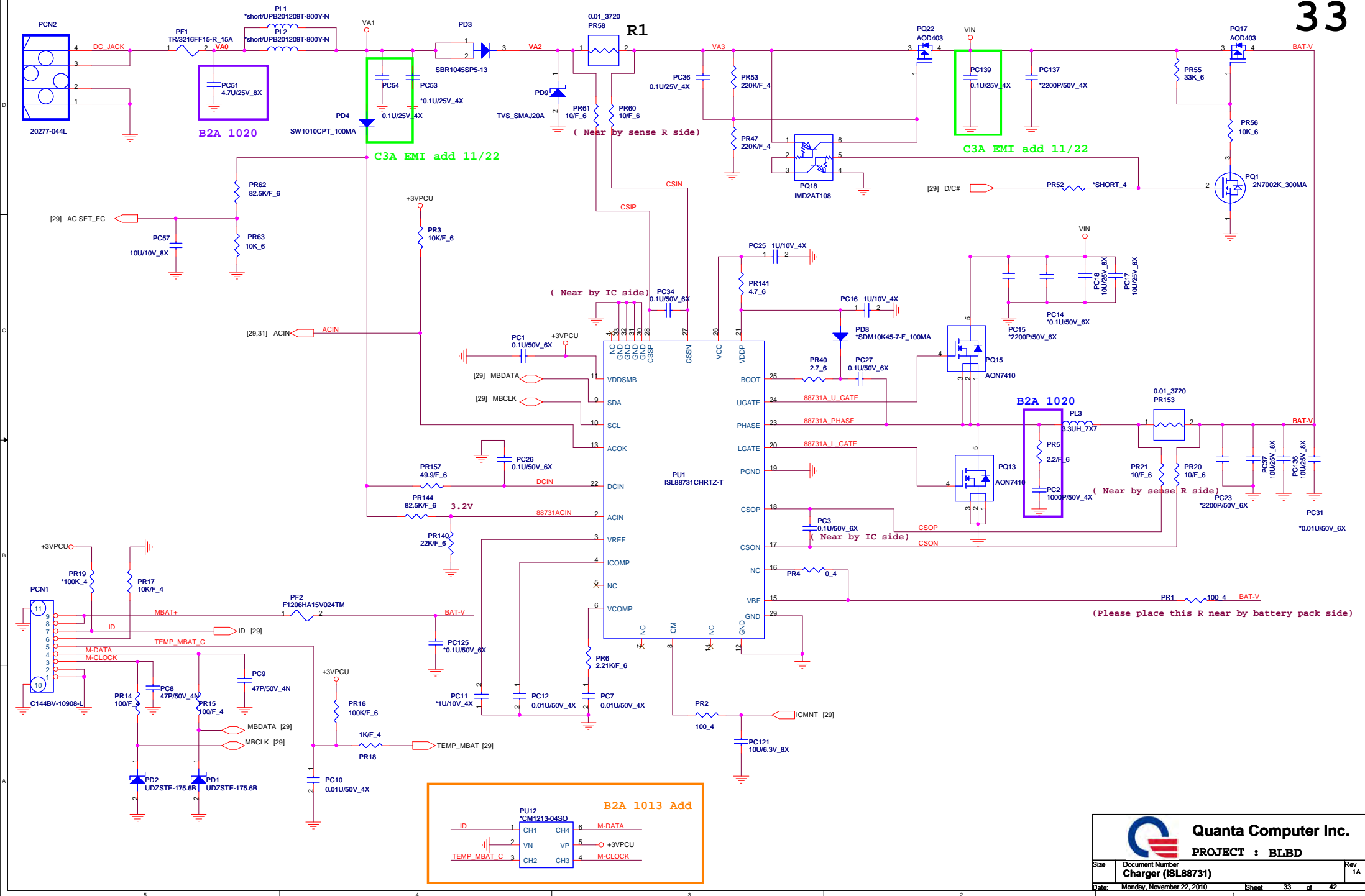
BLANK



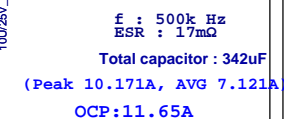
Quanta Computer Inc.

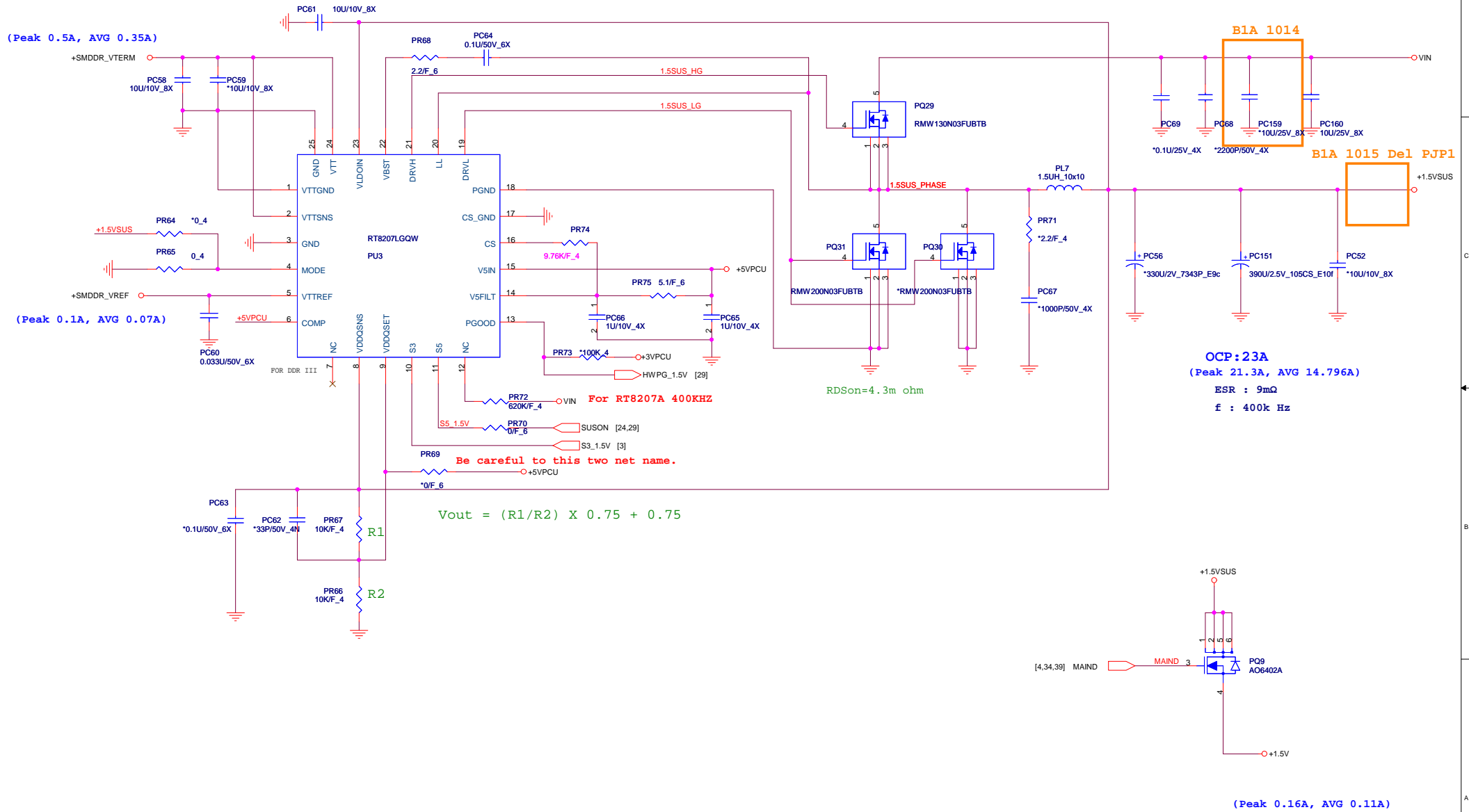
PROJECT : BLBD

Size	Document Number	Rev
	NVRAM Connector	1A
Date:	Monday, November 22, 2010	Sheet 32 of 42



For PM6886 ZD5.6V , 150K/F_4 & 147K/F_4

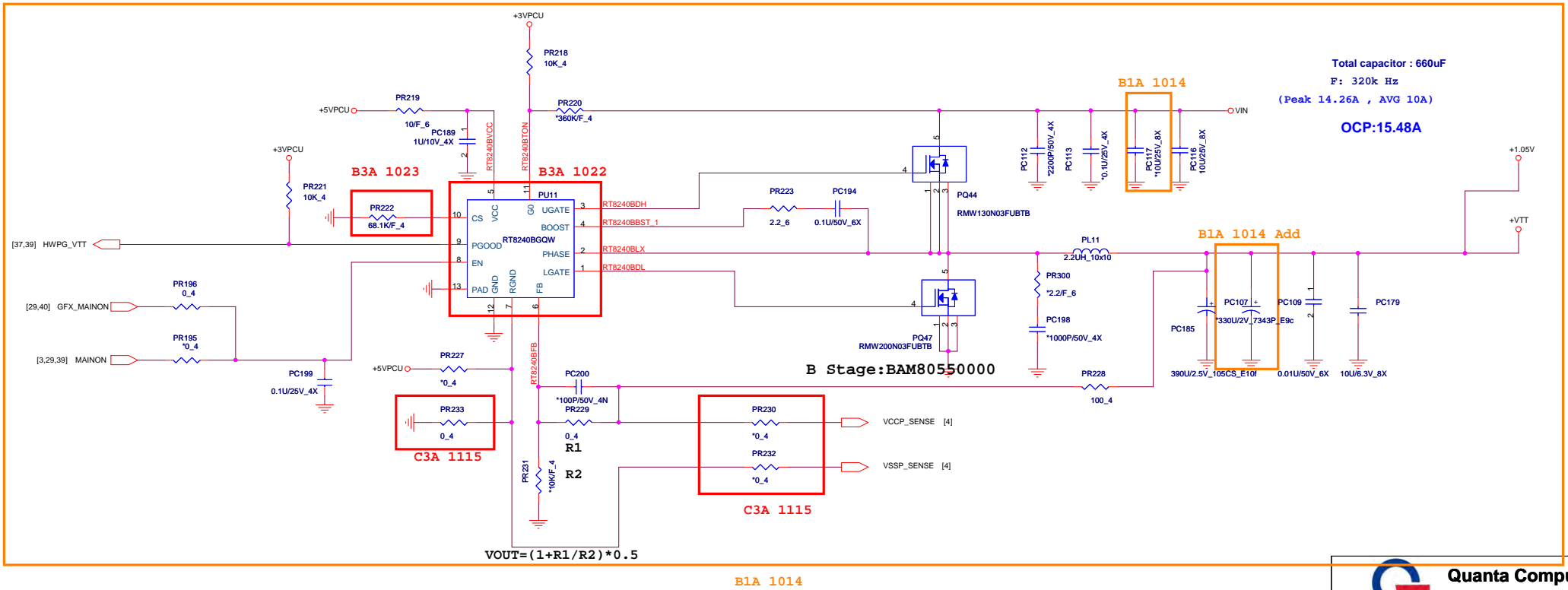


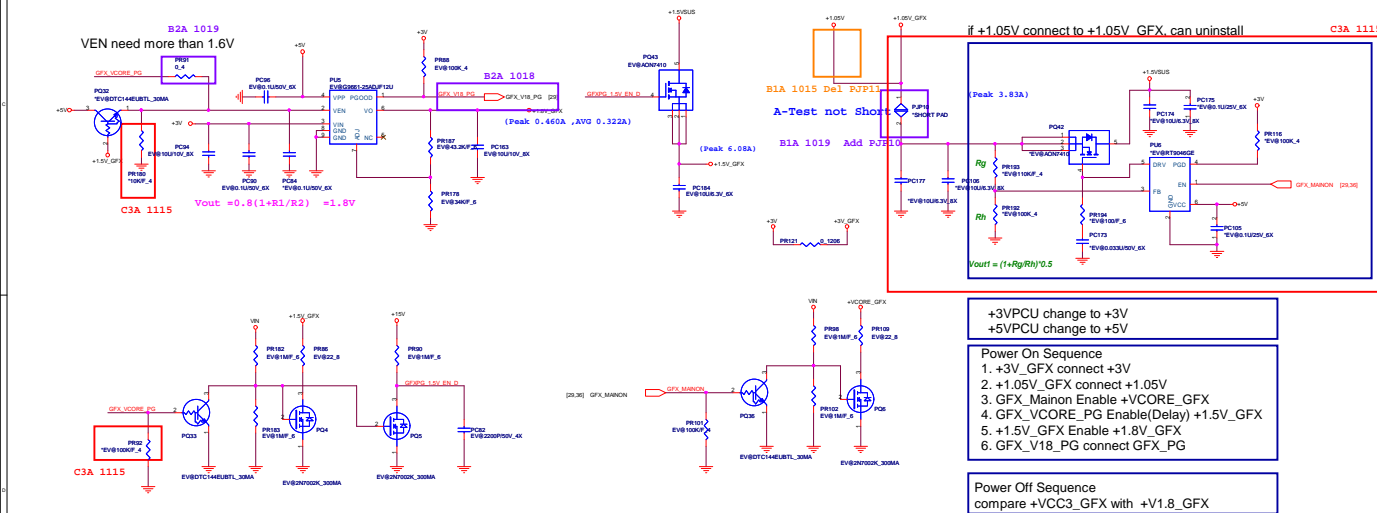
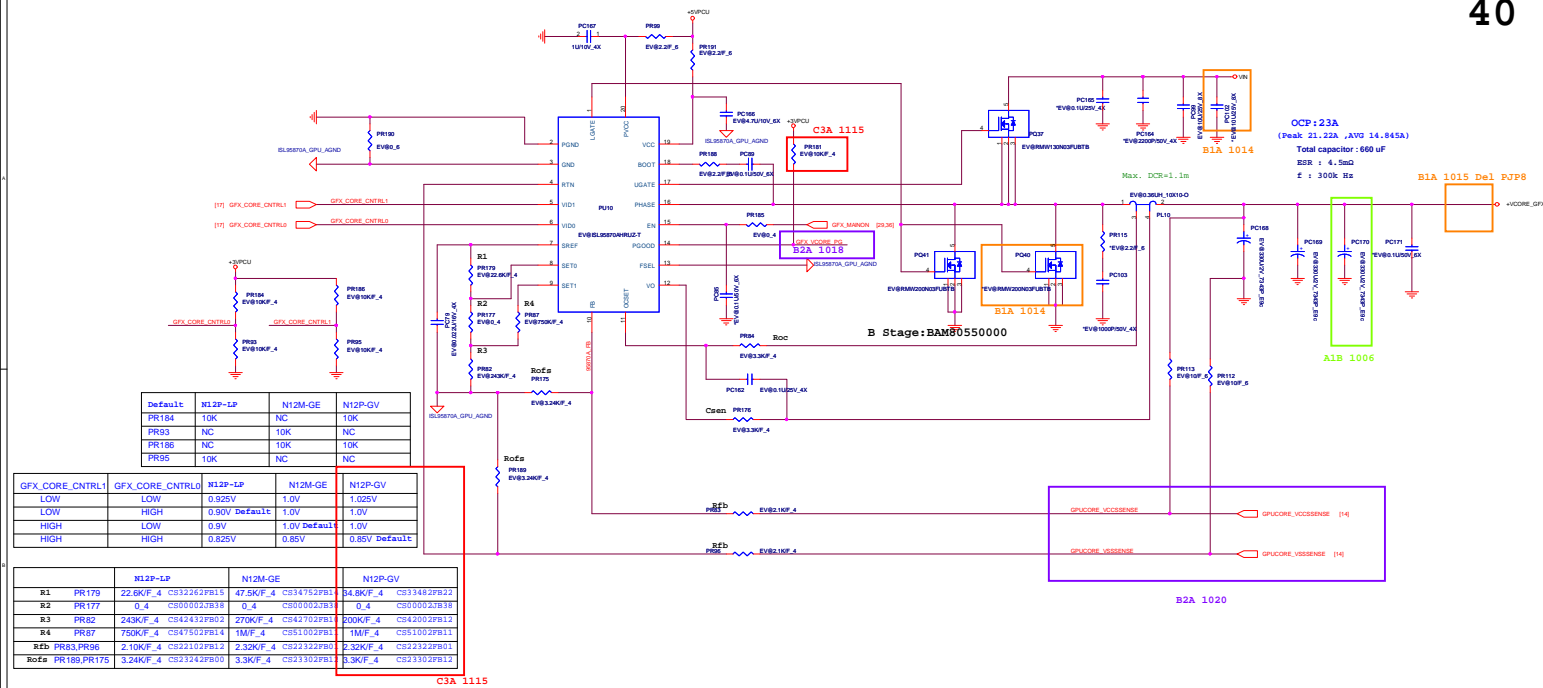


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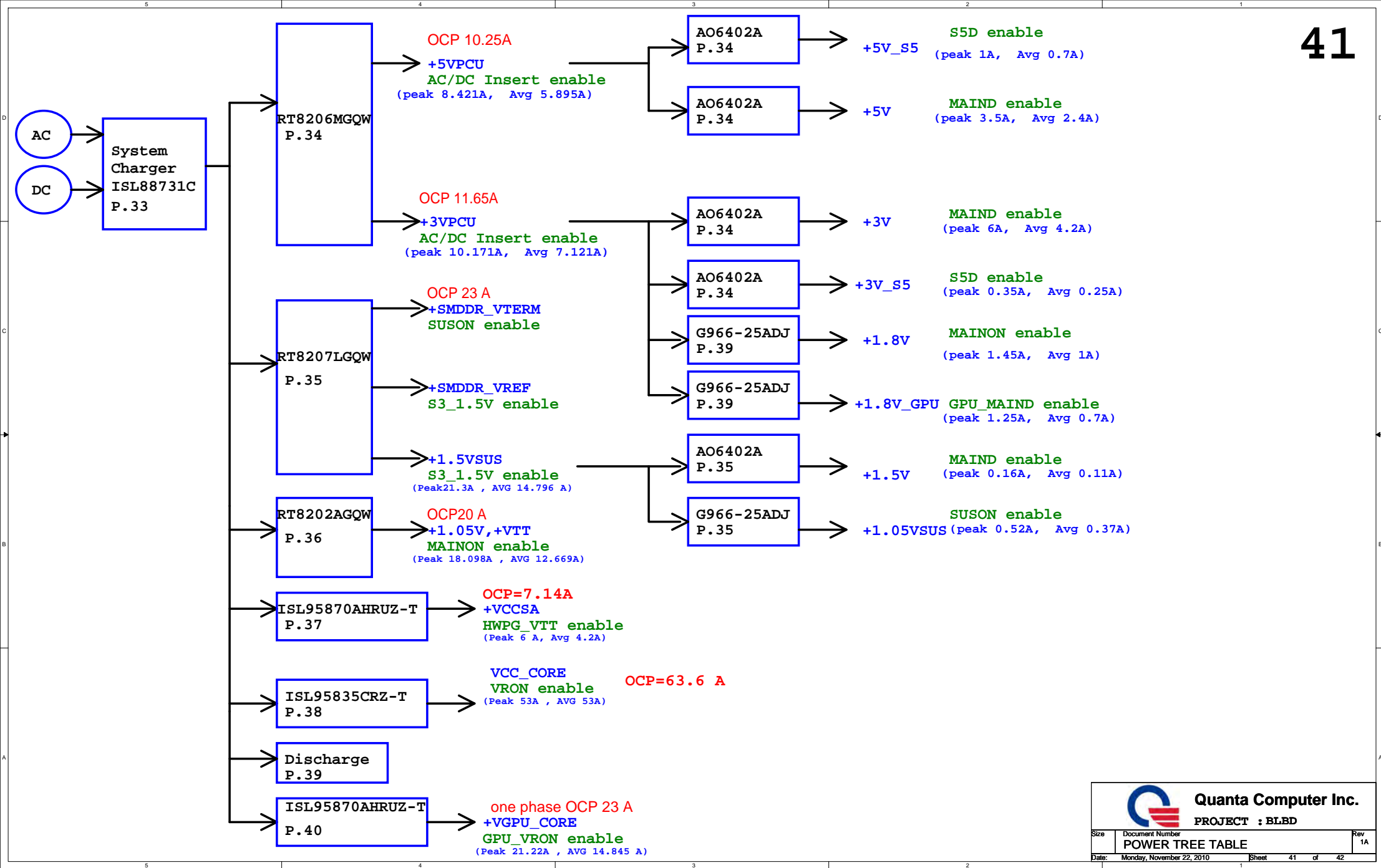
PROJECT : BLBD


Size	Document Number	Rev
	DDR 1.5V(RT8207LGQW)	1A
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- Power On Sequence**
1. +3V_GFX connect +3V
 2. +1.05V_GFX connect +1.05V
 3. GFX_Mainion Enable +VCORE_GFX
 4. GFX_VCORE_PG Enable(Delay) +1.5V_GFX
 5. +1.5V_GFX Enable +1.8V_GFX
 6. GFX_V18_PG connect GFX_PG
- Power Off Sequence**
- compare +VCC3_GFX with +V1.8_GFX



Model		REV	CHANGE LIST				MODEL		BLBD		
							PAGE	FROM	To		
BLBD MB	1A	PAGE 2: Del R19 0 ohm					1	1A			
		PAGE 2: ADD R599 0 ohm, TP81,TP82,TP83,TP84,TP85,TP86,TP87					2	1A			
		PAGE 2: STUFF R385,R394,Q28,C601,R387. NC R386					3	1A			
		PAGE 4: DEL C430, R37, R23, Add C477,C478,C479,C480,C740,C741,C742,C743,C744,C745,C746,R602,R603,R598, Stuff R21					4	1A			
		PAGE 5: ADD TP89, TP1					5	1A			
		PAGE 6: DEL R293, R503, NC R52, ADDR294					6	1A			
		PAGE 8: ADD C750, C751, R601, STUFF R501, NC Q14, Q15					7	1A			
		PAGE 9: DEL R253; R534 CHANGE TO PD					8	1A			
		PAGE 9: CHANGE Board ID9 strap Function name					9	1A			
		PAGE 10: ADD R604					10	1A			
		PAGE 17: CHANGE GPU MULTI level strap select					11	1A			
		PAGE 17: MODIFY GPU STRAP 1 SETTING					12	1A			
		PAGE 22: CHANGE LVDS CN1 FOOTPRINT					13	1A			
		PAGE 23: MINI CARD NC R99, DEL R184					14	1A			
		PAGE 23: ADD Q94,R920 BUT NC, ADD R921 AND MOUNT					15	1A			
		PAGE 25: DEL R68, R49					16	1A			
		PAGE 25: MOUNT C502, C1, C2					17	1A			
		PAGE 26: DEL R368, R369					18	1A			
		PAGE 26: ADD C953 BUT NC					19	1A			
		PAGE 26: ADD C759,C732,C733,C734					20	1A			
		PAGE 27: CHANGE ADOGND TO GND					21	1A			
		PAGE 27: ADD R342 BUT NC					22	1A			
		PAGE 27: NC C735					23	1A			
		PAGE 28: DEL R579, ADD C758					24	1A			
		PAGE 28: ADD R579, R600 PULL 3ND_MBCLK,3ND_MBDATA, NC R197					25	1A			
		PAGE 28: ADD SKU_STRAP1,SKU_STRAP2,SKU_STRAP3					26	1A			
		PAGE 28: CHANGE NET NAME FOR GFX_VCORE_PG TO GFX_V18_PG					27	1A			
		PAGE 31: LED1,LED4,LED5,LED6 change symbol and Foot-print					28	1A			
		PAGE 33: MOUNT PR5,PC2,PC51, ADD PU12 BUT NC					29	1A			
		PAGE 34: CHANGE PU4 TO PM6886					30	1A			
		PAGE 34: NC PR100,PR114,PR208,PR77,PR78, DEL PJP7					31	1A			
		PAGE 35: NC PR159, DEL PJP1,PJP2					32	1A			
		PAGE 36: CHANGE +VTT/+1.05V SCHEMATIC, CHANGE PU11 TO RT8240					33	1A			
		PAGE 37: DEL PJP6					34	1A			
		PAGE 40: DEL PJP8,PJP11, ADD PR91, NC PQ40					35	1A			
		PAGE 28: ADD Q3502					36	1A			
		PAGE 3: Add S3 Power reduction componet R489					37	2A			
		PAGE 31: Delete Card Reader LED componet Q16					38	2A			
		PAGE 31: Add Card Reader LED componet Q3052					39	2A			
		PAGE 8: Add USB_BUS_SW2/3 0 ohm R596,R597					40	2A			
		PAGE 10: Add +VCCAFDI_VRM PD Cap C381					41	2A			
		PAGE 17: Add 15K strap3/4 for GPU R3518,R3534					42	2A			
		PAGE 24: Add common choke for USB EMI solution L73					43	2A			
		PAGE 24: Reserve resistor for USB EMI solution RP24					44	2A			
		PAGE 25: Add ODD Zero power diischarge R614					45	2A			
		PAGE 25: Reserve ODD Zero power diischarge C577					46	2A			
		PAGE 26: Change Value for LAN 51@ to 52@, C95,C96,C100,C102,RN3,RN4					47	2A			
		PAGE 27: Change Card Reader controller U22 source					48	2A			
		PAGE 29: Change MS Strap Power name +3V_PCU to +3VPCU					49	2A			
		PAGE 36: 1.Add PR233 0 ohm PD form Pin7, NC PR230,PR232					50	2A			
		PAGE 38: Change PR155 3.09K to 3.16K, PR159 1.37K to 1.47K, mount PR29,PC19									
		PAGE 38: Change PQ26,PQ27,PQ23,PQ25 RMW200N03FUBTB to TPCA8065-H									
		PAGE 40: Change PR181 to 10K									
		PAGE 40: Change PR181 to 10K,Reserve PR92 100K ,Reserve +1.05 part all material, Reserve PR180 10K									
		PAGE 40: Voltage Setting for N12P-GV									
		PAGE 2: Add R118 R413, reserve R104,R105,Q5 for cost down Q5									
		DOC NO. 204		PROJECT MODEL :	BLBD	APPROVED BY:	Angelo Su	DATE:	2010/10/01	 Quanta Computer Inc. PROJECT : BLBD	
				PART NUMBER:		DRAWING BY:	Angelo Su	REVISION:	1A		
										Change list	
										Date: Monday, November 22, 2010 Sheet 42 of 42	